CrossLink Family

Preliminary **Data Sheet**

FPGA-DS-02007 Version 1.1

March 2017

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CSI	Camera Serial Interface
DSI	Display Serial Interface
EBR	Embedded Block RAM
ECLK	Edge Clock
FPD	Flat Panel Display
I^2C	Inter-Integrated Circuit
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
NVCM	Non-Volatile Configuration Memory
OTP	One Time Programmable
PCLK	Primary Clock
PFU	Programmable Functional Unit
PLL	Phase Locked Loops
PMU	Power Management Unit
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
WLCSP	Wafer Level Chip Scale Packaging

1. General Description

CrossLink™ from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The device is based on Lattice mobile FPGA technology. It combines the extreme flexibility of an FPGA with the low power, low cost and small footprint of an ASIC.

CrossLink supports video interfaces including MIPI® DPI, MIPI DBI, CMOS camera and display interfaces, OpenLDI, FPD-Link, FLATLINK, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SLVS200, SubLVDS, HiSPi and more.

Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for CrossLink. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using CrossLink. Synthesis library support for CrossLink devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the CrossLink device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Interfaces on CrossLink provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays at 4k UHD and beyond.

1.1. Features

- Ultra-low power
  - Sleep Mode Support
  - Normal Operation – From 5 mW to 150 mW
- Ultra small footprint packages
  - 36-ball WLCSP (6 mm^2)
  - 64-ball ucfBGA (12 mm^2)
  - 80-ball ctfBGA (40 mm^2)
  - 81-ball csfBGA (20 mm^2)
- Programmable architecture
  - 5936 LUTs
  - 180 kb block RAM
  - 47 kb distributed RAM
- Two hardened 4-lane MIPI D-PHY interfaces
  - Transmit and receive
  - 6 Gb/s per D-PHY interface
- Programmable source synchronous I/O
  - MIPI D-PHY Rx, LVDS Rx, LVDS Tx, SubLVDS Rx, SLVS200 Rx, HiSPi Rx
  - 1200 Mb/s per I/O
  - Four high-speed clock inputs
- Programmable CMOS I/O
  - LVTTL and LVCMOS
    - 3.3 V, 2.5 V, 1.8 V and 1.2 V (outputs)
  - LVDS, LVCMOS differential I/Os
- Flexible device configuration
  - One Time Programmable (OTP) non-volatile configuration memory
  - Master SPI boot from external flash
    - Dual image booting supported
  - I^2C programming
  - SPI programming
  - TransFR™ I/O for simple field updates
- Enhanced system level support
  - Reveal logic analyzer
  - TraceID for system tracking
  - On-chip hardened I^2C block
- Applications examples
  - 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge
  - 1:2 MIPI DSI Display Interface Bridge
  - MIPI DSI to/from FPD-Link/OpenLDI LVDS Display Interface Bridge
  - MIPI DSI to/from CMOS Display Interface Bridge
  - MIPI CSI-2 to/from CMOS Image Sensor Interface Bridge
  - SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

2. Application Examples

2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge

Figure 2.1 shows the block diagram for the 2:1 MIPI CSI-2 image sensor aggregator bridge. This solution merges image outputs from multiple sensors into a single CSI-2 output to an application processor.

Table 2.1 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting any input encoding, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. Up to 8 image sensor inputs can be aggregated, depending on data rate and number of lanes. For details, refer to FPGA-IPUG-02002, 2:1 MIPI CSI-2 Bridge Soft IP User Guide.

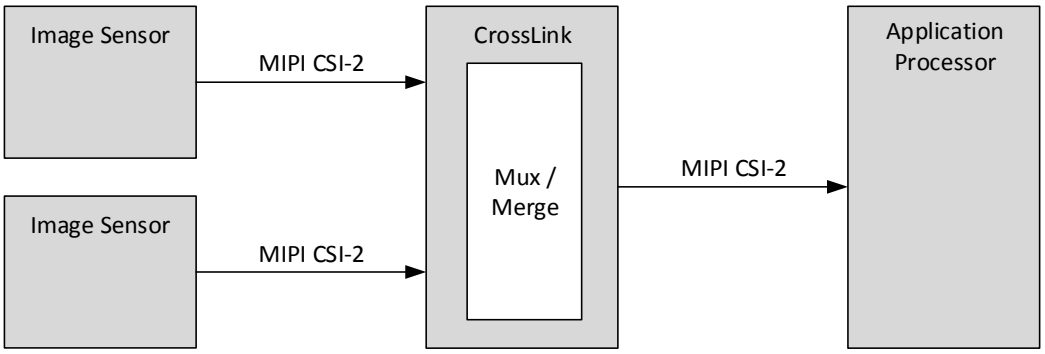


Figure 2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge

Table 2.1. 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge Overview

Application Example Details	
Input Type	2 x 1080p60, 12-bit RAW 2 x 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Programmable Fabric Operation(s)	Merge Image Sensor Outputs with no Frame drop Mux/Merge in flexible combinations
Output Type	1 x 1080p60, 12-bit RAW 1 x 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Additional System Functions	Support for I²C Bridge/Mux for Camera Configuration GPIO for image sensor sync and reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~55 mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~85% of LUT4; ~100% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.2. 1:2 MIPI DSI Display Interface Bridge

Figure 2.2 shows the block diagram for the 1:2 MIPI DSI display interface bridge. This solution duplicates the display output from single application processor DSI output to two different DSI displays.

Table 2.2 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting any input encoding, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. The solution can be customized to split the input image, or perform additional bridging operations. For details, refer to FPGA-IPUG-02001, 1:2 and 1:1 MIPI DSI Display Interface Bridge Soft IP User Guide.

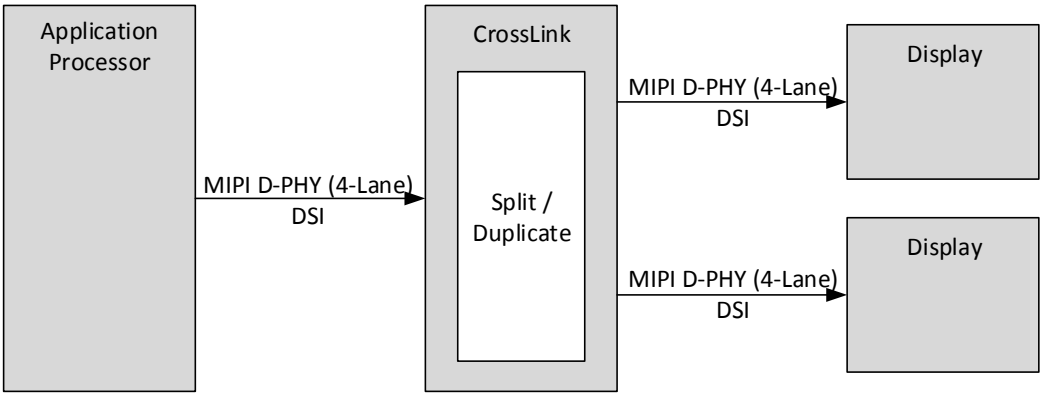


Figure 2.2. 1:2 MIPI DSI Display Interface Bridge

Table 2.2. 1:2 MIPI DSI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Split/Duplicate Image
Output Type	2 x 1080p60, 24-bit RGB 2 x 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~140 mW
Device I/O Used	10 Programmable I/O; 2 x Hard D-PHY Quads
Fabric Resources Used	80% of LUT4; ~80% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.3. FPD-Link/OpenLDI LVDS to MIPI DSI Display Interface Bridge

Figure 2.3 shows the block diagram for the FPD-Link/OpenLDI LVDS to MIPI DSI display interface bridge. This solution bridges the single or dual-channel FPD-Link/OpenLDI LVDS display output from the application processor to a MIPI DSI input display.

Table 2.3 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting both RGB666 and RGB888, variable number of LVDS data lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02005, OpenLDI/FPD-Link/LVDS to MIPI DSI Interface Bridge Soft IP User Guide.

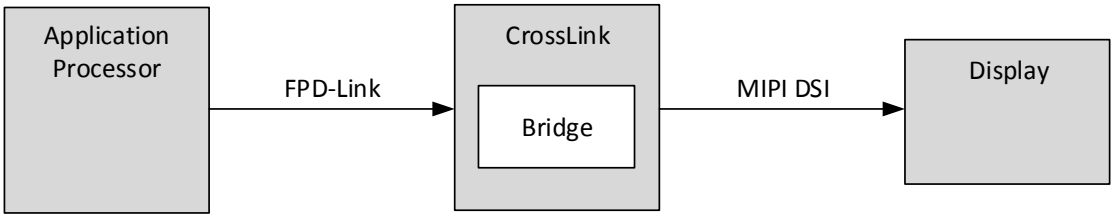


Figure 2.3. FPD-Link/OpenLDI LVDS to MIPI DSI Display Interface Bridge

Table 2.3. FPD-Link/OpenLDI LVDS to MIPI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 2 Channels (2 x 4 Data Lanes and 2 x 1 Clock Lane) @ 74.25 MHz FPD-Link Clock
Programmable Fabric Operation(s)	Bridge
Output Type	1 x 1080p60, 24-bit RGB 1 x 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	TBD mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~50% of LUT4; ~60% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Figure 2.4 shows the block diagram for the MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge. This solution bridges the MIPI DSI output from the application processor to a single or dual channel FPD-Link/OpenLDI LVDS display input.

Table 2.4 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting both RGB666 and RGB888, variable number of LVDS data lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02003, MIPI DSI to OpenLDI/FPD-Link/LVDS Interface Bridge Soft IP User Guide.

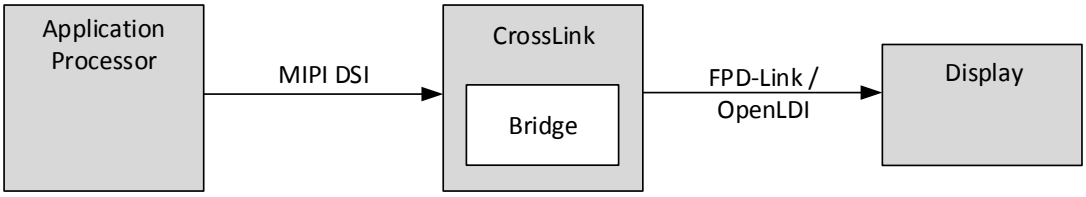


Figure 2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge

Table 2.4. MIPI DSI to FPD-Link/OpenLDI LVDS Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Bridge
Output Type	1080p60, 24-bit RGB 2 Channels (2 x 4 Data Lanes and 2 x 1 Clock Lane) @ 74.25MHz FPD-Link Clock
Additional System Functions	Display Configuration Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	TBD mW
Device I/O Used	20 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~30% of LUT4; ~30% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.5. CMOS to MIPI DSI Display Interface Bridge

Figure 2.5 shows the block diagram for the CMOS to MIPI DSI display interface bridge. This solution bridges the CMOS parallel output from the application processor to a DSI display input.

Table 2.5 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

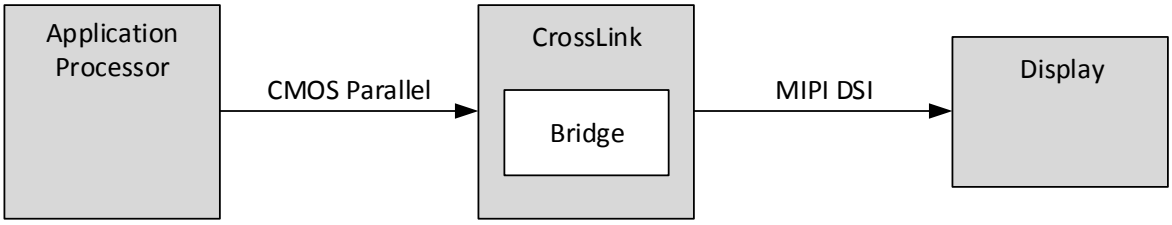


Figure 2.5. CMOS to MIPI DSI Display Interface Bridge

Table 2.5. CMOS to MIPI DSI Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB CMOS Parallel @ 148.5 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Additional System Functions	Display Configuration (DCS) Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~80 mW
Device I/O Used	28 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 2.6 shows the block diagram for the CMOS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges the CMOS parallel output from an image sensor to a CSI-2 input of an application processor.

Table 2.6 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting a wide range of video formats, and data rates up to 150 MHz at the CMOS input side or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02007, CMOS to MIPI D-PHY Interface Bridge Soft IP User Guide.

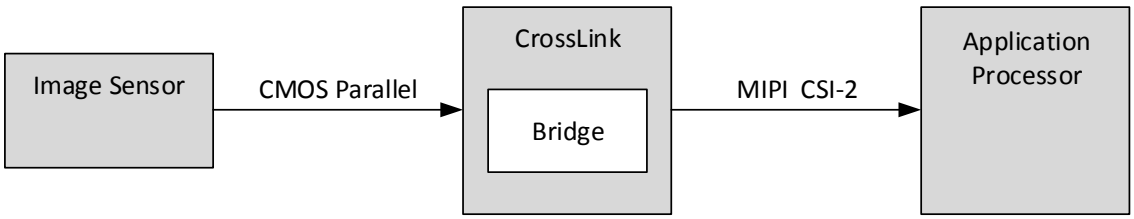


Figure 2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge

Table 2.6. CMOS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 12-bit RAW CMOS Parallel @ 74.25 MHz
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 12-bit RAW 4-Lane MIPI D-PHY @ ~450 Mb/s per lane
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~75 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	~40% of LUT4; ~20% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.7. MIPI DSI to CMOS Display Interface Bridge

Figure 2.7 shows the block diagram for the MIPI DSI to CMOS display interface bridge. This solution bridges the MIPI DSI output from the application processor to CMOS parallel display input.

Table 2.7 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting multiple pixel formats and data rates up to 1.5 Gb/s per lane input and up to 150 MHz CMOS parallel output. For details, refer to FPGA-IPUG-02004, MIPI D-PHY to CMOS Interface Bridge Soft IP User Guide.

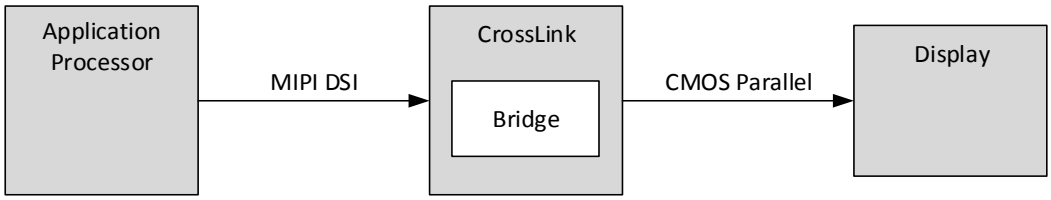


Figure 2.7. MIPI DSI to CMOS Display Interface Bridge

Table 2.7. MIPI DSI to CMOS Display Interface Bridge Overview

Application Example Details	
Input Type	1080p60, 24-bit RGB 4-Lane MIPI D-PHY @ ~900 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, 24-bit RGB CMOS Parallel @ 148.5 MHz
Additional System Functions	Power and Reset Sequencing of Display Backlight PWM Control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~80 mW
Device I/O Used	28 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	15% of LUT4; ~15% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge

Figure 2.8 shows the block diagram for the MIPI DSI to CMOS display interface bridge. This solution bridges the MIPI DSI output from the application processor to CMOS parallel display input.

Table 2.8 provides additional details on the application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting multiple pixel formats and data rates up to 1.5 Gb/s per lane input and up to 150 MHz CMOS parallel output. For details, refer to FPGA-IPUG-02004, MIPI D-PHY to CMOS Interface Bridge Soft IP User Guide.

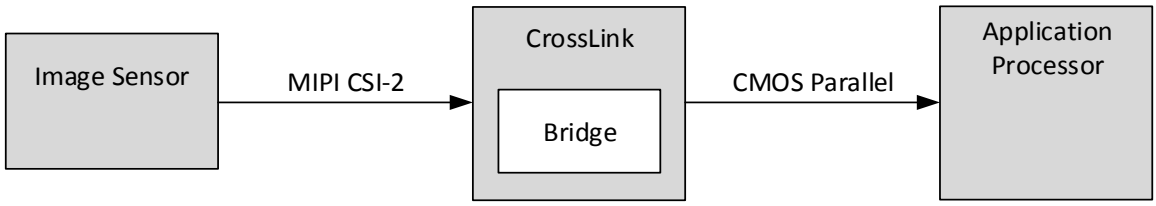


Figure 2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge

Table 2.8. MIPI CSI-2 to CMOS Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	1080p60, RAW12 4-Lane MIPI D-PHY @ ~445 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	1080p60, RAW12 CMOS Parallel @ 74.25 MHz
Additional System Functions	I^2C for Camera Configuration GPIO for image sensor reset/power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	60 mW
Device I/O Used	16 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	15% of LUT4; ~15% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

Figure 2.9 shows the block diagram for a SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge. This solution bridges from an image sensor SubLVDS output to CSI-2 output to an application processor.

Table 2.9 provides additional details for a specific application example, including input and output descriptions and device resource usage. The interface bridge is fully programmable, supporting RAW10 or RAW12 pixel width, variable number of lanes, and data rates up to 1.2 Gb/s per lane input or 1.5 Gb/s per lane output. For details, refer to FPGA-IPUG-02006, SubLVDS to MIPI CSI-2 IP Image Sensor Interface Bridge Soft IP User Guide.

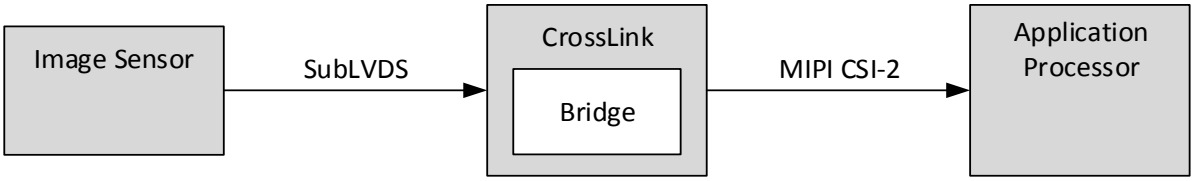


Figure 2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge

Table 2.9. SubLVDS to MIPI CSI-2 Image Sensor Interface Bridge Overview

Application Example Details	
Input Type	4k2k@64.7fps, RAW10 SubLVDS 10 data lane @ 600 Mb/s per lane
Programmable Fabric Operation(s)	Interface Bridge
Output Type	4k2k@64.7fps, RAW10 CSI-2 over 4-Lane MIPI D-PHY @ 1.5 Gb/s per lane
Additional System Functions	Image Frame Control GPIO for reset and power control
Preliminary Example Device Resource Usage*	
Typical Power Consumption	~130 mW
Device I/O Used	22 Programmable I/O; 1 x Hard D-PHY Quads
Fabric Resources Used	80% of LUT4; ~60% of EBR

***Note**: For reference only – exact usage and power consumption depends on specific application parameters. Additional system functions are not included in resource usage. The typical power consumption estimate is based on nominal supply voltages at T_J = 25 °C.

3. Product Feature Summary

Table 3.1 lists CrossLink device information and packages.

Table 3.1. CrossLink Feature Summary

Device	**CrossLink**
LUTs	5936
sysMEM Blocks (9 kb)	20
Embedded Memory (kb)	180
Distributed RAM Bits (kb)	47
General Purpose PLL	1
NVCM	Yes
Embedded I^2C	2
Oscillator (10 KHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2[1, 2]
Packages	**I/O**
36 WLCSP[2] (2.535 × 2.583 mm^2, 0.6 mm)	17
64 ucfBGA (3.5 × 3.5 mm^2, 1 mm)	29
80 ctfBGA (6.5 x 6.5 mm^2, 1 mm)	36
81 csfBGA (4.5 × 4.5 mm^2, 1 mm)	37

Notes:

1. Additional D-PHY Rx interfaces are available using programmable I/O.
2. Only one Hardened D-PHY is available in 36 WLCSP package.

4. Architecture Overview

CrossLink is designed as a flexible, chip-to-chip bridging solution which supports a wide variety of applications, including those described in Application Examples section on page 7.

CrossLink provides three key building blocks for these bridging applications:

- Up to two embedded Hard D-PHY blocks
- Two banks of flexible programmable I/O supporting a variety of standards including D-PHY Rx, subLVDS, SLVS, LVDS, and CMOS
- A programmable logic core providing the LUTs, memory, and system resources to implement a wide range of bridging operations

In addition to these blocks, CrossLink also provides key system resources including a Power Management Unit, flexible configuration interface, additional CMOS GPIO, and user I^2C blocks.

The block diagram for the device is shown in Figure 4.1.

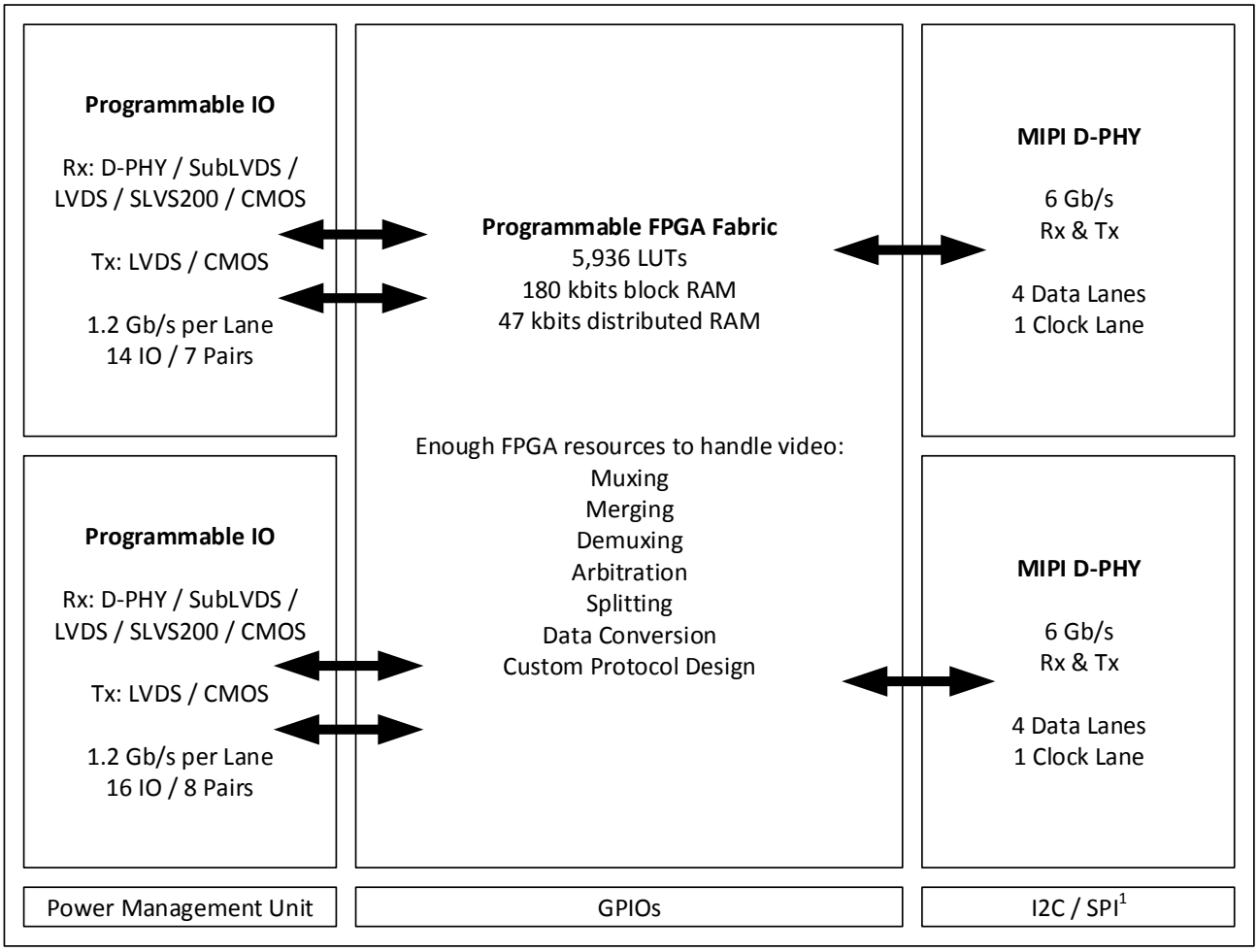


Figure 4.1. CrossLink Device Block Diagram

Note: I^2C and SPI configuration modes are supported. User mode hardened I^2C is also supported.

4.1. MIPI D-PHY Blocks

The top side of the device includes two hard MIPI D-PHY quads. The D-PHY can be configured to support both camera interface (CSI-2) and display interface (DSI) applications. Below is a summary of the features supported by the hard D-PHY quads. Refer to FPGA-TN-02012, CrossLink High-Speed I/O Interface for more information on the Hard D-PHY quads.

- Transmit and Receive compliant to D-PHY Revision 1.1
- High-Speed (HS) and Low-Power (LP) mode support (including built-in contention detect)
- Up to 6 Gb/s per quad (1500 Mb/s data rate per lane)
- Dedicated PLL for Transmit Frequency Synthesis
- Dedicated Serializer and De-Serializer blocks for fabric interfacing
- Supports continuous clock mode or low power clock mode

Lattice Semiconductor provides a set of pre-engineered IP modules which include the full implementation and control of the hard D-PHY blocks for the examples in Application Examples section on page 7, enabling designers to focus on unique aspects of their design.

4.2. Programmable I/O Banks

CrossLink devices provide programmable I/O which can be used to interface to a variety of external standards. The I/O features are summarized below, and described in detail in FPGA-TN-02012, CrossLink High-Speed I/O Interface and FPGA-TN-02016, CrossLink sysI/O Usage Guide. The programmable LVDS/CMOS I/O (Banks 1 and 2) are described below, while the CMOS GPIO (bank 0) and hard D-PHY quads are described separately.

Programmable LVDS/CMOS I/O (Bank 1 and 2) features:

- Built-in support for the following differential standards
  - LVDS – Tx and Rx
  - SLVS – Rx
  - SubLVDS – Rx
  - MIPI – Rx (both LP and HS receive on a single differential pair)
- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs)
  - LVTTL33
- Independent voltage levels per bank based on VCCIO supply
- Input/output gearboxes per LVDS pair supporting several ratios for video interface applications
  - DDRX1, DDRX2, DDRX4, DDRX8 and DDRX71, DDRX141
  - Programmable delay cells to support edge-aligned and center-aligned interfaces
- Programmable differential termination (~ 100 Ω) with dynamic enable control
- Tri-state control for output
- Input/output register blocks
- Single-ended standards support open-drain and programmable input hysteresis
- Optional weak pull-up resistors

To ensure the MIPI Rx interface implemented in FPGA fabric using Programmable I/Os runs in an optimal environment, follow this guideline of assigning I/Os to the bank for the MIPI Rx inputs:

- When an SLVS/MIPI Rx interface is placed in Bank 1 or 2, do not place both Banks 1 and 2 with LVCMOS outputs in these 2 banks.

4.3. Programmable FPGA Fabric

4.3.1. FPGA Fabric Overview

CrossLink is built around a programmable logic fabric consisting of 5936 four input lookup tables (LUT4) arranged alongside dedicated registers in Programmable Functional Units (PFU). These PFU blocks are the building blocks for logic, arithmetic, RAM and ROM functions. The PFU blocks are connected via a programmable routing network. The Lattice Diamond design software configures the PFU blocks and the programmable routing for each unique design. Interspersed between rows of PFU are rows of sysMEM™ Embedded Block RAM (EBR), with programmable I/O banks, embedded I^2C and embedded MIPI D-PHY arranged on the top and bottom of the device as shown in Figure 4.2.

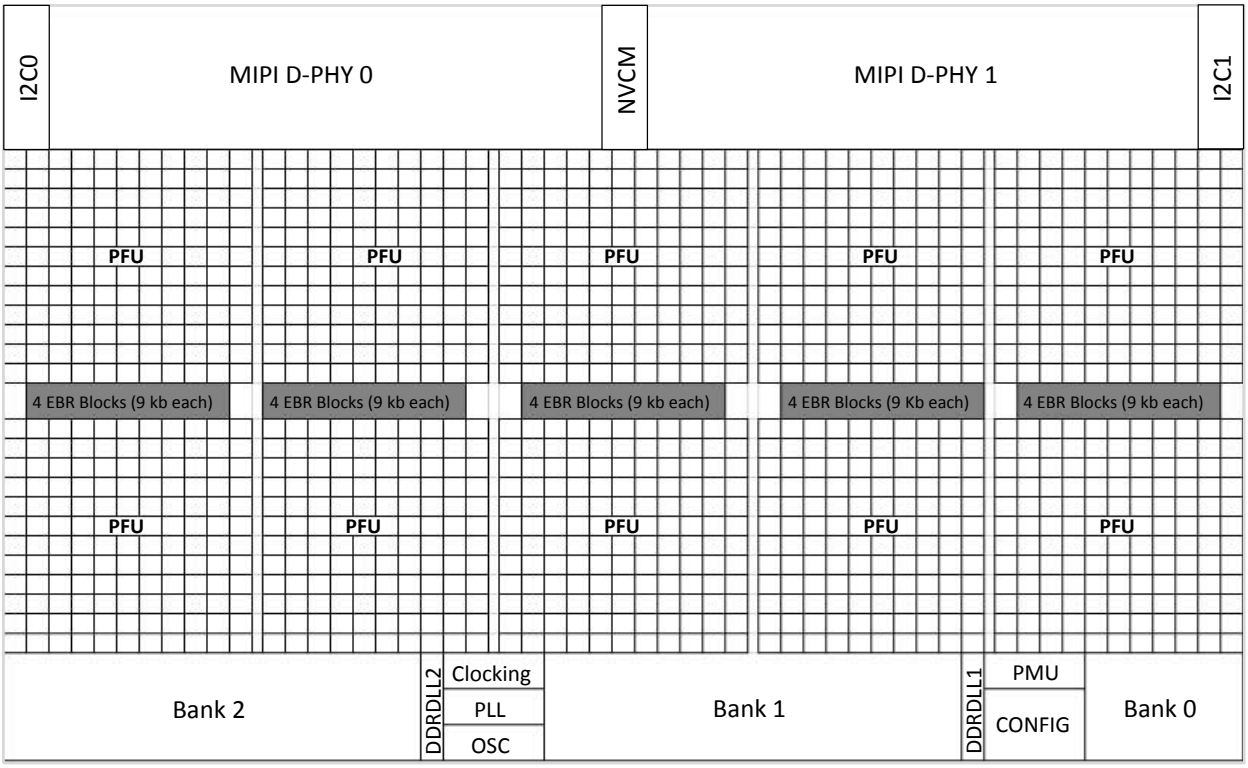


Figure 4.2. CrossLink Device Simplified Block Diagram (Top Level)

4.3.2. Clocking Overview

The CrossLink device family provides resources to support a wide range of clocking requirements for programmable video bridging. These resources are listed below. For details, refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide.

- sysCLOCK PLL
  - Flexible Frequency Synthesis (See Table 5.14 for input frequency range and output frequency range.)
  - Dynamically selectable Clock Input
  - Four Clock Outputs
    - Independent, dynamic enable control
    - Programmable phase adjustment
  - Standby Input
  - Lock Output
- Clock Distribution Network
  - Eight Primary Clocks
    - Dedicated Clock input pins (PCLK)
    - Source from PLL, Clock Divider, Hard D-PHY blocks or On-chip Oscillator

- Four Edge Clocks for high-speed DDR interfaces
  - 2 per Programmable I/O bank
  - Source from PCLK pins, PLL or DLL blocks
  - Programmable Clock divider per Edge Clock
  - Delay primitives for 90 degree phase shifting of clock/data (DDRDLL, DLLDEL)
- Dynamic Clock Control
  - Fabric control to disable clock nets for power savings
- Dynamic Clock Select
  - Smart clock multiplexer with two independent inputs and glitchless output support
- Two On-Chip Oscillators
  - Always-on Low Frequency (LFCLKOUT) with nominal frequency of 10 kHz
  - High-Frequency (HFCLKOUT) with nominal frequency of 48 MHz, programmable output dividers, and dynamic enable control

4.3.3. Embedded Block RAM Overview

CrossLink devices also contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9 kB RAM with memory core, dedicated input registers and output registers with separate clock and clock enable. Supported modes and other general information on the EBR are listed below. For details, refer to FPGA-TN-02017, CrossLink Memory Usage Guide.

- Support for different memory configurations
  - Single Port
  - True Dual Port
  - Pseudo Dual Port
  - ROM
  - FIFO (logic wrapper added automatically by design tools)
- Flexible customization features
  - Initialization of RAM/ROM
  - Memory cascading (handled automatically by design tools)
  - Optional parity bit support
  - Byte-enable
  - Multiple block size options
  - RAM modes support optional Write Through or Read-Before-Write modes

4.4. System Resources

4.4.1. CMOS GPIO (Bank 0)

CrossLink provides dedicated CMOS GPIO on Bank 0 of the device. These GPIO do not include differential signaling support. A summary of the features associated with these GPIOs is listed below:

- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs)
  - LVTTL33
- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 kΩ, 6.8 kΩ, 10 kΩ

4.4.2. Power Management Unit

The embedded Power Management Unit (PMU) allows low-power Sleep State of the device. Figure 4.3 shows the block diagram of the PMU IP.

When instantiated in the design, PMU is always on, and uses the low-speed clock from oscillator of the device to perform its operations.

The typical use case for the PMU is through a user implemented state machine that controls the sleep and wake up of the device. The state machine implemented in the FPGA fabric identifies when the device needs to go into sleep mode, issues the command through PMU's FPGA fabric interface, assigns the parameters for sleep (time to wake up and so on) and issues Sleep command.

The device can be woken up externally using the PMU Wake-Up (USRWKUP) pin, or from the PMU Watch Dog Timer expiry or from I2C0 (address decoding detection or FIFO full in one of hardened I^2C).

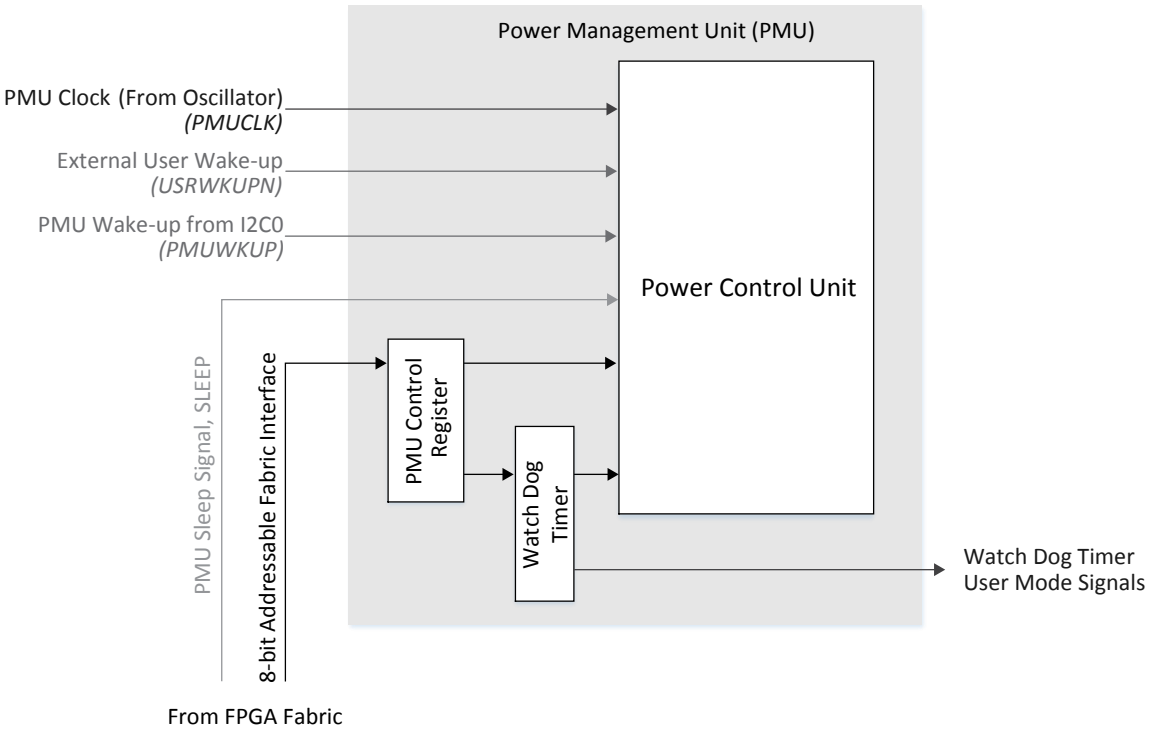


Figure 4.3. CrossLink MIPI D-PHY Block

4.4.2.1. PMU State Machine

PMU can place the device in two mutually exclusive states – Normal State and Sleep State. Figure 4.4 on the next page shows the PMU State Machine triggers for transition from one state to the other.

- Normal state – All elements of the device are active to the extent required by the design. In this state, the device is at fully active and performing as required by the application.
  Note that the power consumption of the device is highest in this state.
- Sleep state – The device is power gated such that the device is not operational. The configuration of the device and the EBR contents are retained; thus in Sleep mode, the device does not lose configuration SRAM and EBR contents. When it transitions to Normal state, device operates with these contents preserved.
  The PMU is active along with the associated GPIOs.
  The power consumption of the device is lowest in this state. This helps reduce the overall power consumption for the device.

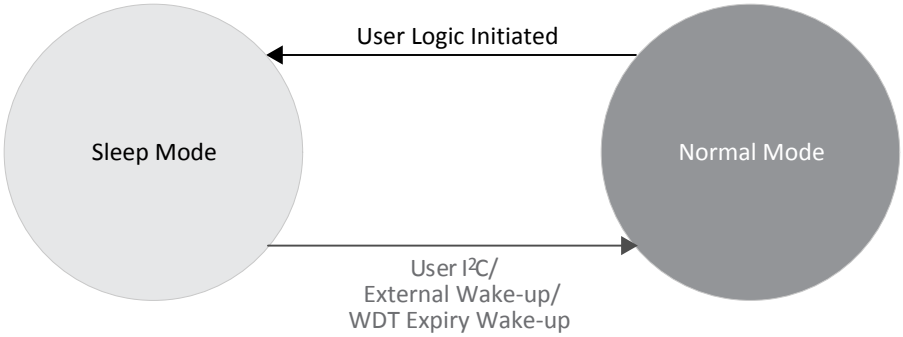


Figure 4.4. CrossLink PMU State Machine

For more details, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

4.4.3. Device Configuration

The CrossLink SRAM can be configured as follows:

- Internal Non Volatile Configuration Memory (NVCM)
  - NVCM can be programmed using either the SPI or I²C port
- Standard Serial Peripheral Interface (Master SPI Mode) Interface to external SPI Flash
- System microprocessor to drive a serial Slave SPI port (SSPI mode)
- System microprocessor to drive a serial Slave I²C port

For more information, refer to FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide. In addition to the flexible configuration modes, the CrossLink configuration engine supports the following special features:

- TransFR (Transparent Field Reconfiguration) allowing users to update logic in field without interrupting system operation by freezing I/O states during configuration
- Dual-Boot Support for primary and golden bitstreams provides automatic recovery from configuration failures
- Security and One-Time Programmable (OTP) modes protect bitstream integrity and prevent readback
- 64-bit unique TraceID per device

4.4.4. User I²C IP

CrossLink devices have two I²C IP cores that can be configured either as an I²C master or as an I²C slave. The I2C0 core has pre-assigned pins, and supports PMU wakeup over I²C. The pins for the I2C1 interface are not pre-assigned – user can use any General Purpose I/O pins.

The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, refer to FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide.

5. DC and Switching Characteristics

5.1. Absolute Maximum Ratings

Table 5.1. Absolute Maximum Ratings[1, 2, 3]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Supply Voltage	–0.5	1.32	V
V_{CCPLL}	PLL Supply Voltage	–0.5	1.32	V
V_{CCAUX}	Auxiliary Supply Voltage for Bank 1, 2 and NVCM	–0.5	2.75	V
V_{CCIO}	I/O Driver Supply Voltage for Banks 0, 1, 2	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CC_DPHY} V_{CCA_DPHY} V_{CCPLL_DPHY} V_{CCMU_DPHY}	MIPI D-PHY Supply Voltages	–0.5	1.32	V
—	Voltage Applied on MIPI D-PHY Pins	–0.5	1.32	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature (TJ)	—	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

5.2. Recommended Operating Conditions

Table 5.2. Recommended Operating Conditions[1, 2]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V
V_{CCAUX}	Auxiliary Supply Voltage for Bank 1, 2 and NVCM	2.375	2.625	V
V_{CCIO}	I/O Driver Supply Voltage for Bank 0, 1, 2	1.14	3.465	V
T_{JIND}	Junction Temperature, Industrial Operation	–40	100	°C
D-PHY External Power Supply				
V_{CC_DPHYx}	Supply Voltage for D-PHY	1.14	1.26	V
V_{CCA_DPHYx}	Analog Supply Voltage for D-PHY	1.14	1.26	V
V_{CCPLL_DPHYx}	PLL Supply voltage for D-PHY	1.14	1.26	V
V_{CCMU_DPHY}	Supply for V_{CC_DPHY1}, V_{CCA_DPHY1} and V_{CCPLL_DPHY1} on the WLCSP36	1.14	1.26	V

Notes:

1. For Correct Operation, all supplies must be held in their valid operation range.
2. Like power supplies, must be tied together if they are at the same supply voltage. Follow the noise filtering recommendations in FPGA-TN-02013, CrossLink Hardware Checklist.

5.3. Preliminary Power Supply Ramp Rates

Table 5.3. Preliminary Power Supply Ramp Rates[1]

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies except V_{CCAUX}	0.6	10	V/ms

Note:

1. Assume monotonic ramp rates.

5.4. Preliminary Power-On-Reset Voltage Levels

Table 5.4. Preliminary Power-On-Reset Voltage Levels[1, 3, 4]

Symbol	Parameter		Min	Typ	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	0.62	0.68	0.93	V
		V_{CCIO0}[2]	0.87	1.08	1.50	V
		V_{CCAUX}	0.90	—	1.53	V
V_{PORDN}	Power-On-Reset ramp down trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	—	—	0.79	V
		V_{CCIO0}[2]	—	—	1.50	V
		V_{CCAUX}	—	—	1.53	V

Notes:

1. These POR ramp up trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. Only V_{CCIO0} (Config Bank) has a Power-On-Reset ramp up trip point. All other VCCIOs do not have Power-On-Reset ramp up detection.
3. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.
4. Configuration starts after V_{CC}, V_{CCIO0} and V_{CCAUX} reach V_{PORUP}. For details, see $t_{REFRESH}$ time in Table 5.21 on page 38.

5.5. ESD Performance

Refer to the LIFMD Product Family Qualification Summary for complete qualification data, including ESD performance.

5.6. Preliminary DC Electrical Characteristics

Over recommended operating conditions.

Table 5.5. Preliminary DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4, 5]	Input or I/O Leakage	$0 \le V_{IN} \le V_{CCIO}$	−10	—	+10	µA
I_{PU}[4]	Internal Pull-Up Current	V_{CCIO} = 1.2 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−2.7	—	−8	µA
		V_{CCIO} = 1.8 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−3	—	−31	µA
		V_{CCIO} = 2.5 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−8	—	−72	µA
		V_{CCIO} = 3.3 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	−11	—	−128	µA
C_1[2]	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf
C_2[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf
V_{HYST}[3]	Hysteresis for Single-Ended Inputs	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	200	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A = 25 °C, f = 1.0 MHz.
3. Hysteresis is not available for V_{CCIO} = 1.2 V.
4. Weak pull-up setting. Programmable pull-up resistors on Bank 0 will see higher current. Refer to FPGA-TN-02016, CrossLink sysI/O Usage Guide for details on programmable pull-up resistors.
5. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO}, or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

5.7. Preliminary CrossLink Supply Current

Over recommended operating conditions.

Table 5.6. Preliminary CrossLink Supply Current

Symbol	Parameter	Typ	Unit
Normal Operation[1]			
I_{CC}	Core Power Supply Current	7.17	mA
I_{CCPLL}	PLL Power Supply Current	0.05	mA
$I_{CCAUX25VPP}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	2.65	mA
I_{CCIOx}	Bank x Power Supply Current (per Bank)	0.06	mA
I_{CCA_DPHYx}	V_{CCA_DPHYx} Power Supply Current	8.33	mA
I_{CCPLL_DPHYx}	V_{CCPLL_DPHYx} Power Supply Current	1.31	mA
Standby Current[2]			
$I_{CCSTDBY}$	Core Power Supply Standby Current	2.73	mA
$I_{CCPLLSTDBY}$	PLL Power Supply Standby Current	—	mA
$I_{CCAUX25VPPSTDBY}$	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Standby Current	0.46	mA
$I_{CCIOSTDBY}$	Bank Power Supply Standby Current (per Bank)	0	mA
$I_{CCA\_DPHYxSTDBY}$	V_{CCA_DPHYx} Power Supply Standby Current	0.01	mA
$I_{CCPLL\_DPHYxSTDBY}$	V_{CCPLL_DPHYx} Power Supply Standby Current	0.01	mA
Sleep/Power Down Mode Current[3]			
I_{CC_SLEEP}	Core Power Supply Sleep Current	0.48	mA
I_{CCGPLL_SLEEP}	PLL Power Supply Current	0.05	mA
I_{CCAUX_SLEEP}	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	0.03	mA
I_{CCIOx_SLEEP}	Bank Power Supply Current (per Bank)	0.06	mA
$I_{CCPLL\_DPHY\_SLEEP}$	V_{CCPLL_DPHY} Power Supply Sleep Current	0.01	mA
$I_{CCA\_DPHY\_SLEEP}$	V_{CCA_DPHY} Power Supply Sleep Current	0.05	mA

Notes:

1. **Normal Operation**
   Typical design as defined in 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge section, under the following conditions:
   a. T_J = 25 °C, all power supplies at nominal voltages.
   b. Typical processed device in csfBGA81 package.
   c. To determine power for all other applications and operating conditions, use Power Calculator in Lattice Diamond design software
2. **Standby Operation**
   A typically processed device in csfBGA81 package with blank pattern programmed, under the following conditions:
   a. All outputs are tri-stated, all inputs are held at either V_{CCIO}, or GND.
   b. All clock inputs are at 0 MHz.
   c. T_J = 25 °C, all power supplies at nominal voltages.
   d. No pull-ups on I/O.
3. **Sleep/Power Down Mode**
   Typical design as defined in 2:1 MIPI CSI-2 Image Sensor Aggregator Bridge section, under following conditions:
   a. Design is put into Sleep/Power Down Mode with user logic powers down D-PHY, and enters into Sleep Mode in PMU.
   b. T_J = 25 °C, all power supplies at nominal voltages.
   c. Typical processed device in csfBGA81 package.
4. **For ucfBGA64 package**
   a. V_{CCA_DPHY0} and V_{CCA_DPHY1} are tied together as V_{CC_DPHYX}.
   b. V_{CCPLL_DPHY0} and V_{CCPLL_DPHY1} are tied together as V_{CC_DPHYX}.
5. **For WLCS36 package**
   a. V_{CCGPLL} and V_{CCIO1} (Bank 1) are tied together to V_{CC}.
   b. V_{CCPLL_DPHY} and V_{CCA_DPHY} are tied together as V_{CCMU_DPHY}.
6. To determine the CrossLink start-up peak current, use the Power Calculator tool in the Lattice Diamond design software.

5.8. Preliminary Power Management Unit (PMU) Timing

Table 5.7. Preliminary PMU Timing[1]

Symbol	Parameter	Device	Max	Unit
$t_{PMUWAKE}$	Time for PMU to wake from Sleep mode	All Devices	1	ms

Note:

1. For details on PMU usage, refer to FPGA-TN-02018, Power Management and Calculation for CrossLink Devices.

5.9. sysI/O Recommended Operating Conditions

Table 5.8. sysI/O Recommended Operating Conditions[1]

Standard	V_{CCIO}		
	Min	Typ	Max
LVCMOS33/LVTTL33	3.135	3.30	3.465
LVCMOS25	2.375	2.50	2.625
LVCMOS18	1.710	1.80	1.890
LVCMOS12 (Output only)	1.140	1.20	1.260
subLDVS (Input only)	2.375	2.50	2.625
SLVS (Input only)[2]	2.375	2.50	2.625
LVDS	2.375	2.50	2.625
MIPI (Input only)	1.140	1.20	1.260

Note:

1. For input voltage compatibility, refer to FPGA-TN-02016, CrossLink sysI/O Usage Guide.
2. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.10. Preliminary sysI/O Single-Ended DC Electrical Characteristics

Table 5.9. Preliminary sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS33/ LVTTL33	–0.3	0.8	2.0	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	8	–8
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS25	–0.3	0.7	1.7	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	6	–6
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	4	–4
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS12 (Output only)	—	—	—	—	0.40	V_{CCIO} – 0.4	2	–2
					0.20	V_{CCIO} – 0.2	0.1	–0.1

5.11. Preliminary sysI/O Differential Electrical Characteristics

5.11.1. Preliminary LVDS/subLVDS/SLVS

Over recommended operating conditions.

Table 5.10. LVDS/subLVDS[1]/SLVS[1, 2]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INPM}	Input Voltage	—	0.00	—	2.40	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference between the two inputs	–100	—	100	mV
$V_{THD(subLVDS)}$	Differential Input Threshold	Difference between the two inputs	–90	—	90	mV
$V_{THD(SLVS)}$	Differential Input Threshold	Difference between the two inputs	TBD	—	TBD	mV
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ω	—	1.43	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ω	0.90	1.08	—	V
V_{OD}	Output Voltage Differential	$\lvert V_{OP} - V_{OM} \rvert$, RT = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset	$(V_{OH} + V_{OL})/2$, RT = 100 Ω	1.13	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V driver outputs shorted to each other	—	—	12	mA

Notes:

1. Inputs only for subLVDS and SLVS.
2. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.11.2. Preliminary Hardened MIPI D-PHY I/Os

Table 5.11. Preliminary MIPI D-PHY

	Description	Min	Typ	Max	Unit
Receiver					
High Speed					
V_{CMRX}	Common-Mode Voltage HS Receive Mode	70	—	330	mV
V_{IDTH}	Differential Input High Threshold	—	—	70	mV
V_{IDTL}	Differential Input Low Threshold	−70	—	—	mV
V_{IHHS}	Single-ended Input High Voltage	—	—	460	mV
V_{ILHS}	Single-ended Input Low Voltage	−40	—	—	mV
$V_{TERM-EN}$	Single-ended Threshold for HS Termination Enable	—	—	450	mV
Z_{ID}	Differential Input Impedance	80	100	125	Ω
Low Power					
V_{IH}	Logic 1 Input Voltage	880	—	—	mV
V_{IL}	Logic 0 Input Voltage, not in ULP State	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 Input Voltage, in ULP State	—	—	300	mV
V_{HYST}	Input Hysteresis	25	—	—	mV
Transmitter					
High Speed					
V_{CMTX}	HS Transmit Static Common Mode Voltage	150	200	250	mV
V_{OD}	HS Transmit Differential Voltage	140	200	270	mV
V_{OHHS}	HS Output High Voltage	—	—	360	mV
Z_{OS}	Single-ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended Output Impedance Mismatch	—	—	10	%
Low Power					
V_{OH}	Output High Level	1.1	1.2	1.3	V
V_{OL}	Output Low Level	−50	—	50	mV
Z_{OLP}	Output Impedance of LP Transmitter	110	—	—	Ω

5.12. Preliminary CrossLink Maximum General Purpose I/O Buffer Speed

Over recommended operating conditions.

Table 5.12. Preliminary CrossLink Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ucfBGA64 packages	600	MHz
	LVDS, V_{CCIO} = 2.5 V, WLCSP36 package	500	MHz
subLVDS	subLVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ucfBGA64 packages	TBD	MHz
	subLVDS, V_{CCIO} = 2.5 V, WLCSP36 package	TBD	MHz
MIPI D-PHY (HS Mode)[6]	MIPI D-PHY, csfBGA81, ctfBGA80, ucfBGA64 packages	600	MHz
	MIPI D-PHY, WLCSP36 package	500	MHz
SLVS	SLVS, VCCIO=2.5 V, csfBGA81, ctfBGA80, ucfBGA64 packages	TBD	MHz
	SLVS, VCCIO=2.5 V, WLCSP36 package	TBD	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	300	MHz
LVCMOS25D	Differential LVCMOS, V_{CCIO} = 2.5 V	300	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	300	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	155	MHz
Maximum Output Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ucfBGA64 packages	600	MHz
	LVDS, V_{CCIO} = 2.5 V, WLCSP36 package	500	MHz
LVTTL33	LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVTTL33D	Differential LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVCMOS33	LVCMOS, 3.3 V	300	MHz
LVCMOS33D	Differential LVCMOS, 3.3 V	300	MHz
LVCMOS25	LVCMOS, 2.5 V	300	MHz
LVCMOS25D	Differential LVCMOS, 2.5 V	300	MHz
LVCMOS18	LVCMOS, 1.8 V	155	MHz
LVCMOS12	LVCMOS, V_{CCIO} = 1.2 V	70	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Table 5.22.
4. Actual system operation may vary depending on user logic implementation.
5. Maximum data rate equals two times the clock rate when utilizing DDR.
6. This is the maximum MIPI D-PHY input rate on the programmable I/O banks 1 and 2. The hardened MIPI D-PHY input and output rates are described in Hardened MIPI D-PHY Performance section. For SLVS/MIPI interface I/O placement, see the Programmable I/O Banks section.

5.13. Preliminary CrossLink External Switching Characteristics

Over recommended commercial operating conditions.

Table 5.13. Preliminary CrossLink External Switching Characteristics[4, 5]

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Clocks					
Primary Clock					
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	150	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	ns
t_{ISKEW_PRI}	Primary Clock Skew Within a Clock	—	—	450	ps
Edge Clock					
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	600	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	0.783	—	ns
t_{ISKEW_EDGE}	Edge Clock Skew Within a Bank	—	—	120	ps
Generic SDR Interface[1]					
General Purpose I/O Pin Parameters Using Clock Tree Without PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	6.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	—	–0.90	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.82	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	—	1.02	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	—	0	—	ns
General Purpose I/O Pin Parameters Using Clock Tree With PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	5.2	ns
t_{SU}	Clock to Data Setup – PIO Input Register	—	0.17	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.01	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	—	1.70	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	—	0	—	ns
Generic DDR Interfaces[2]					
Generic DDRX8 or DDRX4 I/O with Clock and Data Centered at General Purpose Pins (GDDRX8_RX/TX.ECLK.Centered or GDDRX4_RX/TX.ECLK.Centered)					
$t_{SU\_GDDRX4\_8}$	Input Data Set-Up Before CLK Rising and Falling edges	—	0.167	—	ns
$t_{HO\_GDDRX4\_8}$	Input Data Hold After CLK Rising and Falling edges	—	0.167	—	ns
$t_{DVB\_GDDRX4\_8}$	Output Data Valid Before CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	–0.120	—	ns+1/2UI
$t_{DVA\_GDDRX4\_8}$	Output Data Valid After CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s	0.297	—	ns
		Other Data Rates	–0.120	—	ns+1/2UI
$f_{MAX\_GDDRX4\_8}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz

Table 5.13. Preliminary CrossLink External Switching Characteristics (*Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDRX8 or DDRX4 I/O with Clock and Data Aligned at General Purpose Pins (GDDRX8_RX/TX.ECLK.Aligned or GDDRX4_RX/TX.ECLK.Aligned)					
$t_{DVA\_GDDRX4\_8}$	Input Data Valid After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s	—	0.188	ns
		Other Data Rates	—	–0.229	ns+1/2UI
$t_{DVE\_GDDRX4\_8}$	Input Data Hold After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s	0.646	—	ns
		Other Data Rates	0.229	—	ns+1/2UI
$t_{DIA\_GDDRX4\_8}$	Output Data Invalid After CLK Rising and Falling edges Output	—	—	0.120	ns
$t_{DIB\_GDDRX4\_8}$	Output Data Invalid Before CLK Output Rising and Falling edges	—	—	0.120	ns
$f_{MAX\_GDDRX4\_8}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz
General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
$t_{SU\_GDDRX\_MP}$	Input Data Set-Up Before CLK	—	0.167	—	ns
$t_{HO\_GDDRX\_MP}$	Input Data Hold After CLK	—	0.167	—	ns
$f_{MAX\_GDDRX\_MP}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz
Generic DDRX71 or DDRX141 Inputs (GDDRX71_RX.ECLK or GDDRX141_RX.ECLK)					
t_{RPBi_DVA}	Input Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.3	UI
		—	—	–0.222	ns+ (i+ 1/2)*UI
t_{RPBi_DVE}	Input Hold Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.7	—	UI
		—	0.222	—	ns+ (i+ 1/2)*UI
f_{MAX_RX71}	DDR71/DDR141 ECLK Frequency[3]	—	—	450	MHz
Generic DDRX71 Outputs with Clock and Data Aligned at Pin (GDDRX71_TX.ECLK)					
T_{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.143	ns+i*UI
T_{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	–0.143	—	ns+ (i+ 1)*UI
$T_{TPBi\_skew\_UI}$	Tx skew in UI	—	—	0.15	UI
f_{MAX_TX71}	DDR71 ECLK Frequency[3]	csfBGA81	—	525	MHz
		WLCSP36	—	500	MHz

Table 5.13. Preliminary CrossLink External Switching Characteristics (*Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDRX141 Outputs with Clock and Data Aligned at Pin (GDDRX141_TX.ECLK)					
T_{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	All Devices	—	0.125	ns+i*UI
T_{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	All Devices	–0.125	—	ns+(i+ 1)*UI
$T_{TPBi\_skew\_UI}$	TX skew in UI	All Devices	—	0.15	UI
f_{MAX_TX141}	DDR141 ECLK Frequency[3]	csfBGA81	—	600	MHz
		WLCSP36	—	500	MHz

Notes:
1. General I/O timing numbers based on LVCMOS 2.5, 0 pf load.
2. Generic DDRX8, DDRX71 and DDRX141 timing numbers based on LVDS I/O.
3. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
4. These numbers are generated using best case PLL located.
5. All numbers are generated with the Lattice Diamond design software.

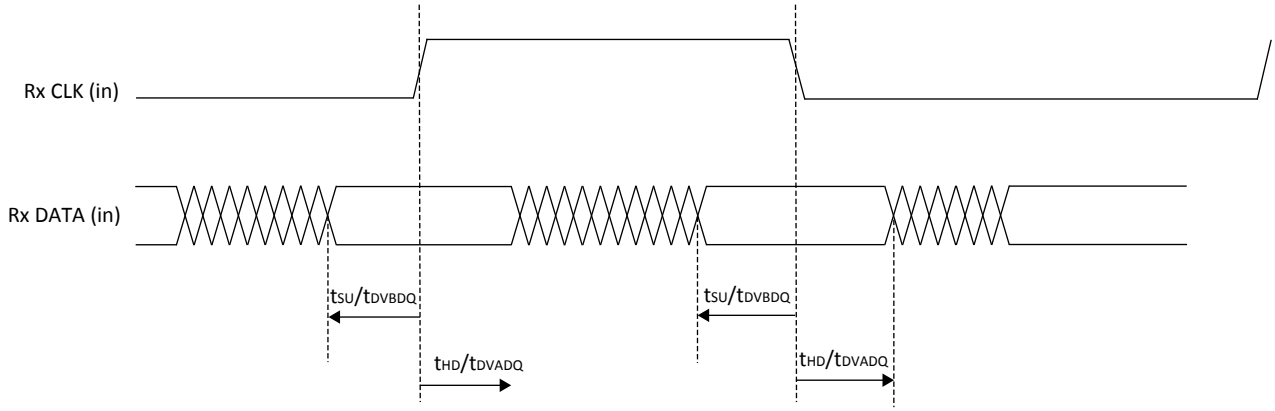


Figure 5.1. Receiver RX.CLK.Centered Waveforms

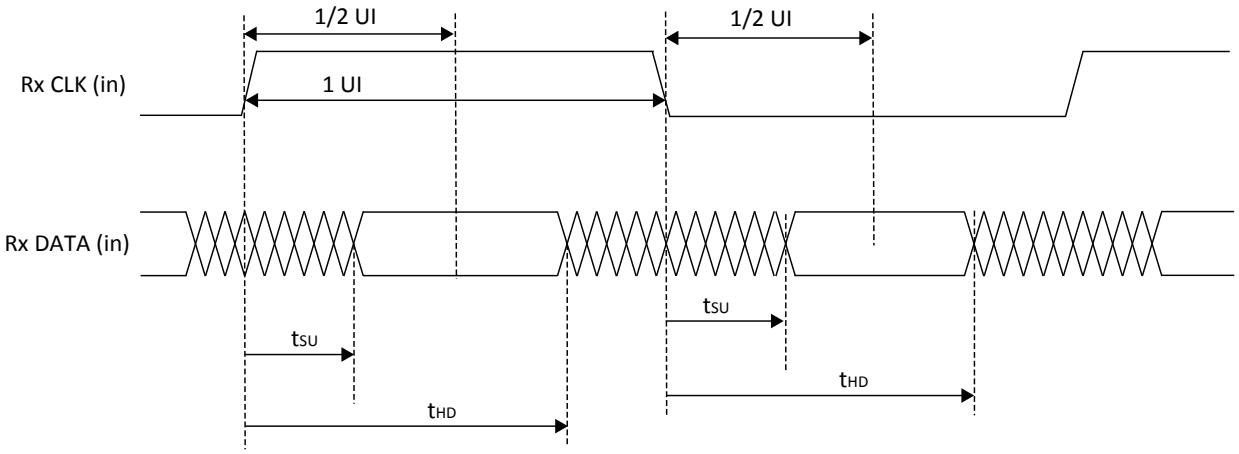


Figure 5.2. Receiver RX.CLK.Aligned Input Waveforms

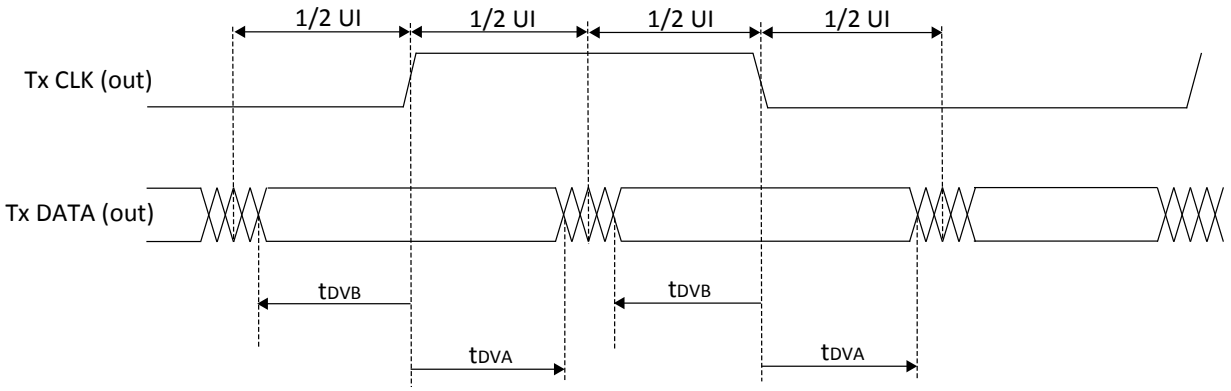


Figure 5.3. Transmit TX.CLK.Centered Output Waveforms

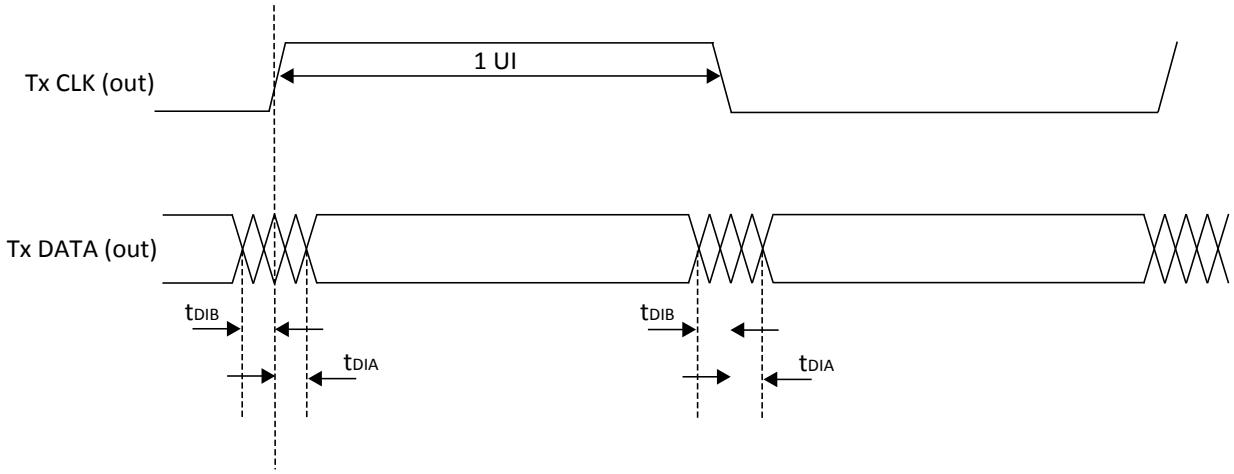


Figure 5.4. Transmit TX.CLK.Aligned Waveforms

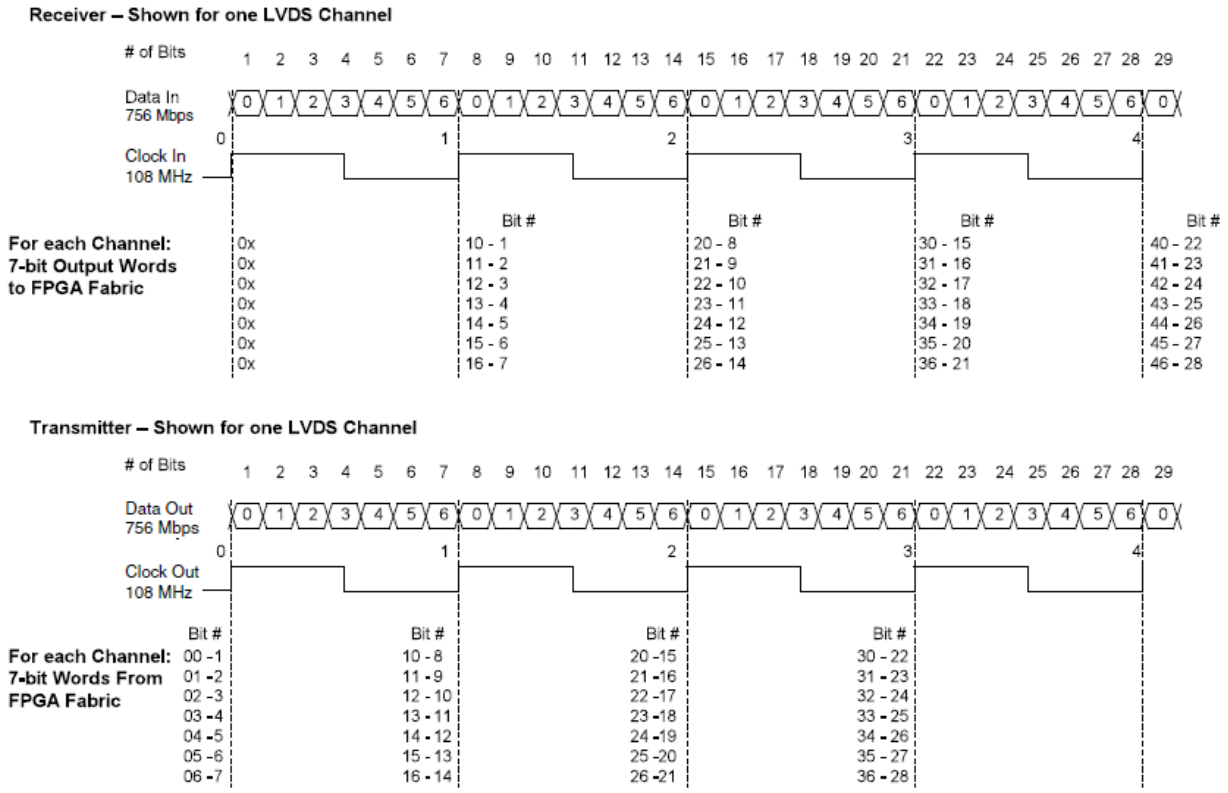


Figure 5.5. DDRX71, DDRX141 Video Timing Waveforms

5.14. Preliminary sysCLOCK PLL Timing

Over recommended operating conditions.

Table 5.14. Preliminary sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	10	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	4.6875	600	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH4}	Output Phase Accuracy	—	–5	5	%
t_{OPJIT}[1]	Output Clock Period Jitter[3]	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter[3]	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	UIPP
	Output Clock Phase Jitter	$f_{PFD} > 100$ MHz	—	200	ps p-p
		$f_{PFD} < 100$ MHz	—	0.05	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_{LOCK}[2]	PLL Lock-in Time	—	—	1	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	500	ps p-p
		$f_{PFD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns

Notes:

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PFD} \geq 10$ MHz. For $f_{PFD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

5.15. Hardened MIPI D-PHY Performance

Table 5.15. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s)[1]

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX8}	Input Data Setup before CLK	0.133	—	ns
t_{HO_MIPIX8}	Input Data Hold after CLK	0.133	—	ns
t_{DVB_MIPIX8}	Output Data Valid before CLK Output	0.200	—	ns
t_{DVA_MIPIX8}	Output Data Valid after CLK Output	0.200	—	ns

Note:

1. For WLCSP36 package, the MIPI D-PHY f_{max} is 1200 Mb/s, for other packages, f_{max} is 1500 Mb/s.

Table 5.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX4}	Input Data Setup before CLK	0.150	—	ns
t_{HO_MIPIX4}	Input Data Hold after CLK	0.150	—	ns
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.250	—	ns
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.250	—	ns

Table 5.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX4}	Input Data Setup before CLK	0.167	—	ns
t_{HO_MIPIX4}	Input Data Hold after CLK	0.167	—	ns
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.350	—	ns
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.350	—	ns

5.16. Preliminary Internal Oscillators (HFOSC, LFOSC)

Table 5.18. Preliminary Internal Oscillators

Parameter	Parameter Description	Min	Typ	Max	Unit
f_{CLKHF}	HFOSC CLKK Clock Frequency	43.2	48	52.8	MHz
f_{CLKLF}	LFOSC CLKK Clock Frequency	9	10	11	kHz
DCH_{CLKHF}	HFOSC Duty Cycle (Clock High Period)	45	—	55	%
DCH_{CLKLF}	LFOSC Duty Cycle (Clock High Period)	45	—	55	%

5.17. Preliminary User I²C[1]

Table 5.19. Preliminary User I²C[1]

Symbol	Parameter	STD Mode		FAST Mode		FAST Mode Plus[2]		Units
		Min	Max	Min	Max	Min	Max	
f_{scl}	SCL Clock Frequency	—	100	—	400	—	1000[2]	kHz

Notes:

1. Refer to the I²C Specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I²C bus. Internal pull up may not be sufficient to support the maximum speed.

5.18. CrossLink sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 5.20. CrossLink sysCONFIG Port Timing Specifications

Symbol	Parameter	Min	Max	Unit
All Configuration Mode				
t_{PRGM}	CRESETB LOW Pulse Accepted	145	—	ns
Slave SPI				
f_{CCLK}	SPI_SCK Input Clock Frequency	—	110	MHz
t_{STSU}	MOSI Setup Time	0.5	—	ns
t_{STH}	MOSI Hold Time	2.0	—	ns
t_{STCO}	SPI_SCK Falling Edge to Valid MISO Output	—	13.3	ns
t_{SCS}	Chip Select HIGH Time	42	—	ns
t_{SCSS}	Chip Select Setup Time	0.5	—	ns
t_{SCSH}	Chip Select Hold Time	0.5	—	ns
Master SPI				
f_{CCLK}	MCK Output Clock Frequency	—	52.8	MHz
I^2C*				
f_{MAX}	Maximum SCL Clock Frequency (Fast-Mode Plus	—	1	MHz

***Note**: Refer to the I^2C specification for timing requirements when configuring with I^2C port.

5.19. Preliminary SRAM Configuration Time from NVCM

Over recommended operating conditions.

Table 5.21. Preliminary SRAM Configuration Time from NVCM

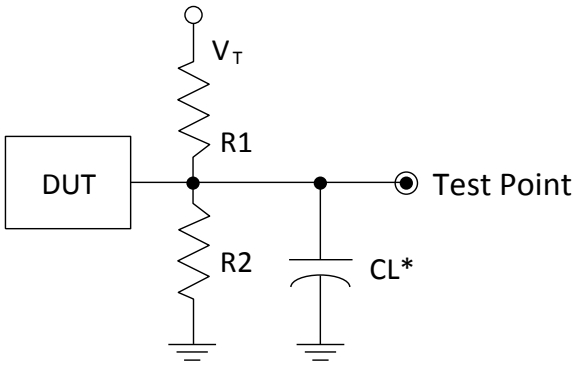
Symbol	Parameter	Typ	Unit
$t_{CONFIGURATION}$	POR to Device I/O Active[1]	83	ms

Note:

1. Before and during configuration, the I/Os are held in tristate with weak internal pullups enabled. I/Os are released to user functionality when the device has finished configuration.

5.20. Switching Test Conditions

Figure 5.6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 5.22.



*CL Includes Test Fixture and Probe Capacitance

Figure 5.6. Output Test Load, LVTTL and LVCMOS Standards

Table 5.22. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	$V_{OH} - 0.10$	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	$V_{OL} + 0.10$	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

6. Pinout Information

6.1. WLCSP36 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	GNDMU_DPHY1	GND	—	—
A2	VCCMU_DPHY1	DPHY1	—	—
A3	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
A4	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
A5	VCCAUX	VCCAUX	—	—
A6	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B3	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	PB16D	2	PCLKC2_1	Comp_OF_PB16C
B6	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
C1	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
C2	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
C3	PB52	0	SPI_SS/CSN/SCL	—
C4	VCC	VCCAUX	—	—
C5	PB16C	2	PCLKT2_1	True_OF_PB16D
C6	GND	GND	—	—
D1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
D2	PB48	0	PCLKT0_1/USER_SCL	—
D3	PB47	0	PCLKT0_0/USER_SDA	—
D4	CRESET_B	0	—	—
D5	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D6	PB6B	2	—	Comp_OF_PB6A
E1	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
E2	VCCIO0	0	—	—
E3	GND	GND	—	—
E4	PB50	0	MOSI	—
E5	PB16A	2	PCLKT2_0	True_OF_PB16B
E6	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F1	PB51	0	MISO	—
F2	PB49	0	PMU_WKUPN/CDONE	—
F3	PB53	0	SPI_SCK/MCK/SDA	—
F4	PB12A	2	GPLLT2_0	True_OF_PB12B
F5	PB12B	2	GPLLC2_0	Comp_OF_PB12A
F6	VCCIO2	2	—	—

6.2. ucfBGA64 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
A5	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A6	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
A7	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A8	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
B2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
B3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B4	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B5	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B6	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
B7	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
B8	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
C1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
C2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
C3	PB47	0	PCLKT0_0/USER_SDA	—
C4	VCCPLL_DPHYX	DPHY	—	—
C5	VCCA_DPHYX	DPHY	—	—
C6	GNDA_DPHYX	GND	—	—
C7	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
C8	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
D1	PB34B	1	—	Comp_OF_PB34A
D2	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D3	PB52	0	SPI_SS/CSN/SCL	—
D4	GND	GND	—	—
D5	VCC	VCC	—	—
D6	VCCAUX	VCCAUX	—	—
D7	PB16A	2	PCLKT2_0	True_OF_PB16B
D8	PB12A	2	GPLLT2_0	True_OF_PB12B
E1	PB51	0	MISO	—
E2	CRESET_B	0	—	—
E3	PB48	0	PCLKT0_1/USER_SCL	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—
E7	PB16B	2	PCLKC2_0	Comp_OF_PB16A
E8	PB12B	2	GPLLC2_0	Comp_OF_PB12A
F1	PB53	0	SPI_SCK/MCK/SDA	—
F2	PB50	0	MOSI	—

ucfBGA64 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
F3	VCCIO0	0	—	—
F4	VCCIO1	1	—	—
F5	GND	GND	—	—
F6	VCCIO2	2	—	—
F7	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F8	PB6B	2	—	Comp_OF_PB6A
G1	PB38D	1	—	Comp_OF_PB38C
G2	PB38C	1	—	True_OF_PB38D
G3	PB49	0	PMU_WKUPN/CDONE	—
G4	VCCGPLL	VCCGPLL	—	—
G5	PB29B	1	PCLKC1_0	Comp_OF_PB29A
G6	PB29A	1	PCLKT1_0	True_OF_PB29B
G7	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
G8	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
H1	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
H2	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
H3	PB29C	1	PCLKT1_1	True_OF_PB29D
H4	PB29D	1	PCLKC1_1	Comp_OF_PB29C
H5	PB16D	2	PCLKC2_1	Comp_OF_PB16C
H6	PB16C	2	PCLKT2_1	True_OF_PB16D
H7	PB12D	2	—	Comp_OF_PB12C
H8	PB12C	2	—	True_OF_PB12D

6.3. ctfBGA80 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
A2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
A3	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A4	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
A5	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
A9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
A10	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
B1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
B2	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B3	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
B4	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B5	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
B9	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B10	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C1	VSS	GND	—	—
C2	VSSA_DPHY1	DPHY1	—	—
C9	VSSA_DPHY0	DPHY0	—	—
C10	VSS	GND	—	—
D1	PB48	0	PCLKT0_1/USER_SCL	—
D2	VCCPLL_DPHY1	DPHY1	—	—
D4	VCCA_DPHY1	DPHY1	—	—
D5	VCCAUX	VCCAUX	—	—
D6	VSSPLL_DPHYX	GND	—	—
D7	VCCPLL_DPHY0	DPHY0	—	—
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
D10	PB16B	2	PCLKC2_0	Comp_OF_PB16A
E1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
E2	PB34B	1	—	Comp_OF_PB34A
E4	VCC	VCC	—	—
E5	VSS	GND	—	—
E6	VCC	VCC	—	—
E7	VCCA_DPHY0	DPHY0	—	—
E9	PB12A	2	GPLLT2_0	True_OF_PB12B
E10	PB12B	2	GPLLC2_0	Comp_OF_PB12A
F1	PB38A	1	—	True_OF_PB38B
F2	PB38B	1	—	Comp_OF_PB38A

ctfBGA80 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
F4	VCCIO0	0	—	—
F5	VCCIO1	1	—	—
F6	VCCIO2	2	—	—
F7	VCCIO2	2	—	—
F9	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F10	PB6B	2	—	Comp_OF_PB6A
G1	PB50	0	MOSI	—
G2	VSS	GND	—	—
G4	VCCIO1	1	—	—
G5	VSS	GND	—	—
G6	VCCGPLL	VCCGPLL	—	—
G7	VSSGPLL	GND	—	—
G9	PB2A	2	—	True_OF_PB2B
G10	PB2B	2	—	Comp_OF_PB2A
H1	PB52	0	SPI_SS/CSN/SCL	—
H2	CRESET_B	0	—	—
H9	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
H10	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
J1	PB53	0	SPI_SCK/MCK/SDA	—
J2	PB49	0	PMU_WKUPN/CDONE	—
J3	PB43D	1	—	Comp_OF_PB43C
J4	PB38D	1	—	Comp_OF_PB38C
J5	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
J6	PB29D	1	PCLKC1_1	Comp_OF_PB29C
J7	PB29A	1	PCLKT1_0	True_OF_PB29B
J8	PB16D	2	PCLKC2_1	Comp_OF_PB16C
J9	PB6D	2	—	Comp_OF_PB6C
J10	PB6C	2	—	True_OF_PB6D
K1	PB51	0	MISO	—
K2	PB47	0	PCLKT0_0/USER_SDA	—
K3	PB43C	1	—	True_OF_PB43D
K4	PB38C	1	—	True_OF_PB38D
K5	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
K6	PB29C	1	PCLKT1_1	True_OF_PB29D
K7	PB29B	1	PCLKC1_0	Comp_OF_PB29A
K8	PB16C	2	PCLKT2_1	True_OF_PB16D
K9	PB12D	2	—	Comp_OF_PB12C
K10	PB12C	2	—	True_OF_PB12D

6.4. csfBGA81 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
A4	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A5	VCCA_DPHY1	DPHY1	—	—
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A9	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
B3	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	GNDPLL_DPHYX	GND	—	—
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
C1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
C2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
C3	GNDA_DPHY1	DPHY1	—	—
C4	VCCPLL_DPHY1	DPHY1	—	—
C5	GND	GND	—	—
C6	VCCPLL_DPHY0	DPHY0	—	—
C7	GNDA_DPHY0	DPHY0	—	—
C8	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C9	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
D1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D2	PB34B	1	—	Comp_OF_PB34A
D3	VCCA_DPHY1	DPHY1	—	—
D4	GND	GND	—	—
D5	VCCAUX	VCCAUX	—	—
D6	GND	GND	—	—
D7	VCCA_DPHY0	DPHY0	—	—
D8	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
E1	PB38A	1	—	True_OF_PB38B
E2	PB38B	1	—	Comp_OF_PB38A
E3	VCC	VCC	—	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—

csfBGA81 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
E7	PB12B	2	GPLLC2_0	Comp_OF_PB12A
E8	PB6B	2	—	Comp_OF_PB6A
E9	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F1	PB50	0	MOSI	—
F2	PB48	0	PCLKT0_1/USER_SCL	—
F3	VCCIO1	1	—	—
F4	GND	GND	—	—
F5	GNDGPLL	GND	—	—
F6	VCCIO2	2	—	—
F7	PB12A	2	GPLLT2_0	True_OF_PB12B
F8	PB2B	2	—	Comp_OF_PB2A
F9	PB2A	2	—	True_OF_PB2B
G1	PB52	0	SPI_SS/CSN/SCL	—
G2	CRESET_B	0	—	—
G3	VCCIO0	0	—	—
G4	VCCIO1	1	—	—
G5	VCCGPLL	VCCGPLL	—	—
G6	PB29B	1	PCLKC1_0	Comp_OF_PB29A
G7	PB29A	1	PCLKT1_0	True_OF_PB29B
G8	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
G9	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
H1	PB53	0	SPI_SCK/MCK/SDA	—
H2	PB49	0	PMU_WKUPN/CDONE	—
H3	PB43D	1	—	Comp_OF_PB43C
H4	PB38D	1	—	Comp_OF_PB38C
H5	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
H6	PB29D	1	PCLKC1_1	Comp_OF_PB29C
H7	PB16D	2	PCLKC2_1	Comp_OF_PB16C
H8	PB6D	2	—	Comp_OF_PB6C
H9	PB6C	2	—	True_OF_PB6D
J1	PB51	0	MISO	—
J2	PB47	0	PCLKT0_0/USER_SDA	—
J3	PB43C	1	—	True_OF_PB43D
J4	PB38C	1	—	True_OF_PB38D
J5	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
J6	PB29C	1	PCLKT1_1	True_OF_PB29D
J7	PB16C	2	PCLKT2_1	True_OF_PB16D
J8	PB12D	2	—	Comp_OF_PB12C
J9	PB12C	2	—	True_OF_PB12D

6.5. Dual Function Pin Descriptions

The following table describes the dual functions available to certain pins on the CrossLink device. These pins may alternatively be used as general purpose I/O when the described dual function is not enabled.

Signal Name	I/O	Description
General Purpose		
USER_SCL	I/O	User Slave I2C0 clock input and Master I²C0 clock output. Enables PMU wake-up via I2C0.
USER_SDA	I/O	User Slave I2C0 data input and Master I²C0 data output. Enables PMU wakeup via I2C0.
PMU_WKUPN	—	This pin wakes the PMU from sleep mode when toggled low.
Clock Functions		
GPLL2_0[T, C]_IN	I	General Purpose PLL (GPLL) input pads: T = true and C = complement. These pins can be used to input a reference clock directly to the General Purpose PLL. These pins do not provide direct access to the primary clock network.
GR_PCLK[Bank]0	I	These pins provide a short General Routing path to the primary clock network. Refer to FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide for details.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins provide direct access to the primary and edge clock networks.
MIPI_CLK[T/C][Bank]_0	I/O	MIPI D-PHY Reference CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins can be used to input a reference clock directly to the D-PHY PLLs. These pins do not provide direct access to the primary clock network.
Configuration		
CDONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. Holding CDONE delays configuration.
SPI_SCK	I	Input Configuration Clock for configuring CrossLink in Slave SPI mode (SSPI).
MCK	O	Output Configuration Clock for configuring CrossLink in Master SPI mode (MSPI).
SPI_SS	I	Input Chip Select for configuring CrossLink in Slave SPI mode (SSPI).
CSN	O	Output Chip Select for configuring CrossLink in Master SPI mode (MSPI).
MOSI	I/O	Data Output when configuring CrossLink in Master SPI mode (MSPI), data input when configuring CrossLink in Slave SPI mode (SSPI).
MISO	I/O	Data Input when configuring CrossLink in Master SPI mode (MSPI), data output when configuring CrossLink in Slave SPI mode (SSPI).
SCL	I/O	Slave I²C clock I/O when configuring CrossLink in I²C mode.
SDA	I/O	Slave I²C data I/O when configuring CrossLink in I²C mode.

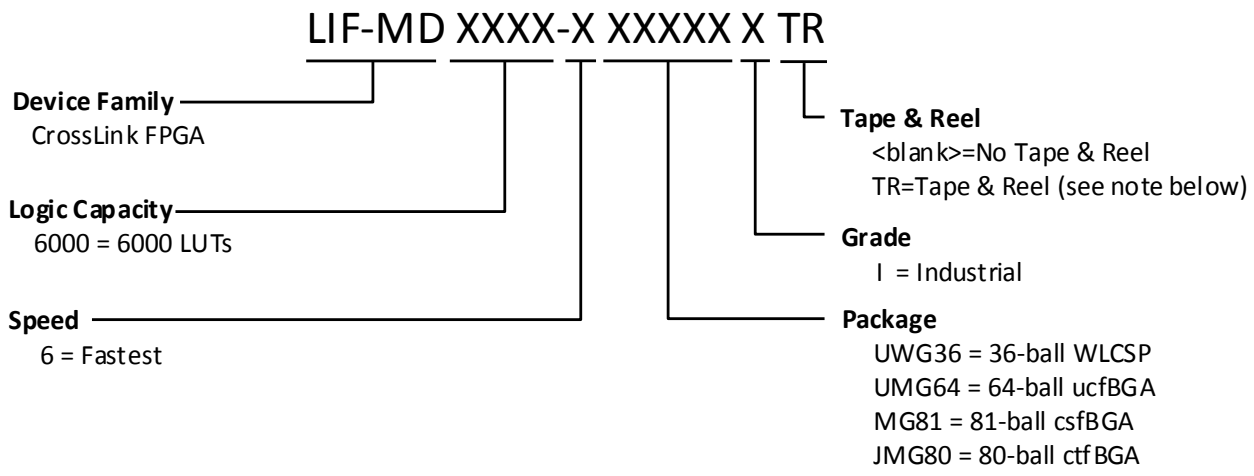
6.6. Dedicated Function Pin Descriptions

Signal Name	I/O	Description
Configuration		
CRESET_B	I	Configuration Reset, active LOW.
MIPI D-PHY		
DPHY[num]_CK[P/N]	I/O	MIPI D-PHY Clock [num] = D-PHY 0 or 1, P = Positive, N = Negative.
DPHY[num]_D[P/N][lane]	I/O	MIPI D-PHY Data [num] = D-PHY 0 or 1, P = Positive, N = Negative, Lane = data lane in the D-PHY block 0, 1, 2 or 3.

6.7. Pin Information Summary

Pin Type	CrossLink			
	WLCSP36	ucfBGA64	ctfBGA80	csfBGA81
General Purpose I/O per Bank				
Bank 0	7	6	7	7
Bank 1	0	10	14	14
Bank 2	10	12	16	16
Total General Purpose Single Ended IO	**17**	**28**	**37**	**37**
Differential I/O pairs per Bank				
Bank 0	0	0	0	0
Bank 1	0	5	7	7
Bank 2	5	6	8	8
Total General Purpose Differential I/O pairs	5	11	15	15
D-PHY	1	2	2	2
D-PHY Clock/Data	10	20	20	20
D-PHY VCC	1	2	4	4
D-PHY GND	1	1	3	3
VCC/VCCIOx/VCCAUX/VCCGPLL	4	8	9	10
GND	3	4	9	9
CRESETB	1	1	1	1
Total Balls	**36**	**64**	**80**	**81**

7. CrossLink Part Number Description



7.1. Ordering Part Numbers

Industrial

Part Number	Grade	Package	Pins	Temp.	LUTs (K)
LIF-MD6000-6UWG36ITR	–6	Lead free WLCSP	36	Industrial	5.9
LIF-MD6000-6UMG64I	–6	Lead free ucfBGA	64	Industrial	5.9
LIF-MD6000-6MG81I	–6	Lead free csfBGA	81	Industrial	5.9
LIF-MD6000-6JMG80I	–6	Lead free ctfBGA	80	Industrial	5.9

Note: UWG36 package is available in shipments of 5000 pieces/reel (TR), 1000 pieces/reel (TR1K), and 50 pieces/reel (TR50 – for samples only).

References

For more information, refer to the following technical notes:

- FPGA-TN-02012, CrossLink High-Speed I/O Interface
- FPGA-TN-02013, CrossLink Hardware Checklist
- FPGA-TN-02014, CrossLink Programming and Configuration Usage Guide
- FPGA-TN-02015, CrossLink sysCLOCK PLL/DLL Design and Usage Guide
- FPGA-TN-02016, CrossLink sysI/O Usage Guide
- FPGA-TN-02017, CrossLink Memory Usage Guide
- FPGA-TN-02018, Power Management and Calculation for CrossLink Devices
- FPGA-TN-02019, CrossLink I2C Hardened IP Usage Guide
- FPGA-TN-02020, Advanced CrossLink I2C Hardened IP Reference Guide

For package information, refer to the following technical notes:

- TN1074, PCB Layout Recommendations for BGA Packages
- TN1076, Solder Reflow Guide for Surface Mount Devices
- TN1242, Wafer-Level Chip-Scale Package Guide
- Thermal Management
- Package Diagrams

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- MIPI Standards (D-PHY): www.mipi.org

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
March 2017	1.1	Updated I/O placements on banks containing MIPI interface in Programmable I/O Banks section. Updated DC and Switching Characteristics section: • Updated Table 5.4. Preliminary Power-On-Reset Voltage Levels1, [3, 4], added row of V_{PORDN} • Added Note 5 to Table 5.5. Preliminary DC Electrical Characteristics • Updated Table 5.6. Preliminary CrossLink Supply Current, added notes • Updated max values of V_{THD} and $V_{THD(subLVDS)}$ in Table 5.10. LVDS/subLVDS1/SLVS1, [2] • Maximum input frequency values of subLVDS and SLVS are TBD in Table 5.12. Preliminary CrossLink Maximum I/O Buffer Speed • Updated Table 5.13. Preliminary CrossLink External Switching Characteristics4, [5] • Updated min values of t_{SU_MIPIX4} and t_{HO_MIPIX4} in Table 5.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s) and Table 5.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s) • Updated Table 5.20. CrossLink sysCONFIG Port Timing Specifications • Updated Table 5.21. Preliminary SRAM Configuration Time from NVCM Updated Pinout Information section Updated CrossLink Part Number Description
July 2016	1.0	Updated document numbers.
May 2016	1.0	First preliminary release.

7TH Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com