DATA SHEET

TDA8569Q
4 × 40 W BTL quad car radio power amplifier

Product specification
Supersedes data of 1997 Mar 27

2003 Aug 08

Philips Semiconductors

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4 × 40 W BTL quad car radio power amplifier

TDA8569Q

FEATURES

- Capable of driving 2 Ω loads
- Requires very few external components
- High output power
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit safe to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Pin compatible with the TDA8567Q.

GENERAL DESCRIPTION

The TDA8569Q is an integrated class-B output amplifier in a 23-lead Single-In-Line (SIL) plastic power package. It contains four amplifiers in Bridge-Tied Load (BTL) configuration, each with a gain of 26 dB. The output power is 4 × 40 W in a 2 Ω load.

APPLICATIONS

- The device is developed primarily for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	230	–	mA
I_{stb}	standby current		–	0.2	10	μA
I_{sw}	switch-on current		–	–	80	μA
$\|Z_i\|$	input impedance		25	30	–	kΩ
P_o	output power	THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_S = 0 Ω	–	60	–	dB
α_{cs}	channel separation	R_S = 10 kΩ	–	55	–	dB
G_v	closed loop voltage gain		25	26	27	dB
$V_{n(o)}$	noise output voltage	R_S = 0 Ω	–	–	120	μV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8569Q	DBS23P	plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)	SOT411-1

BLOCK DIAGRAM

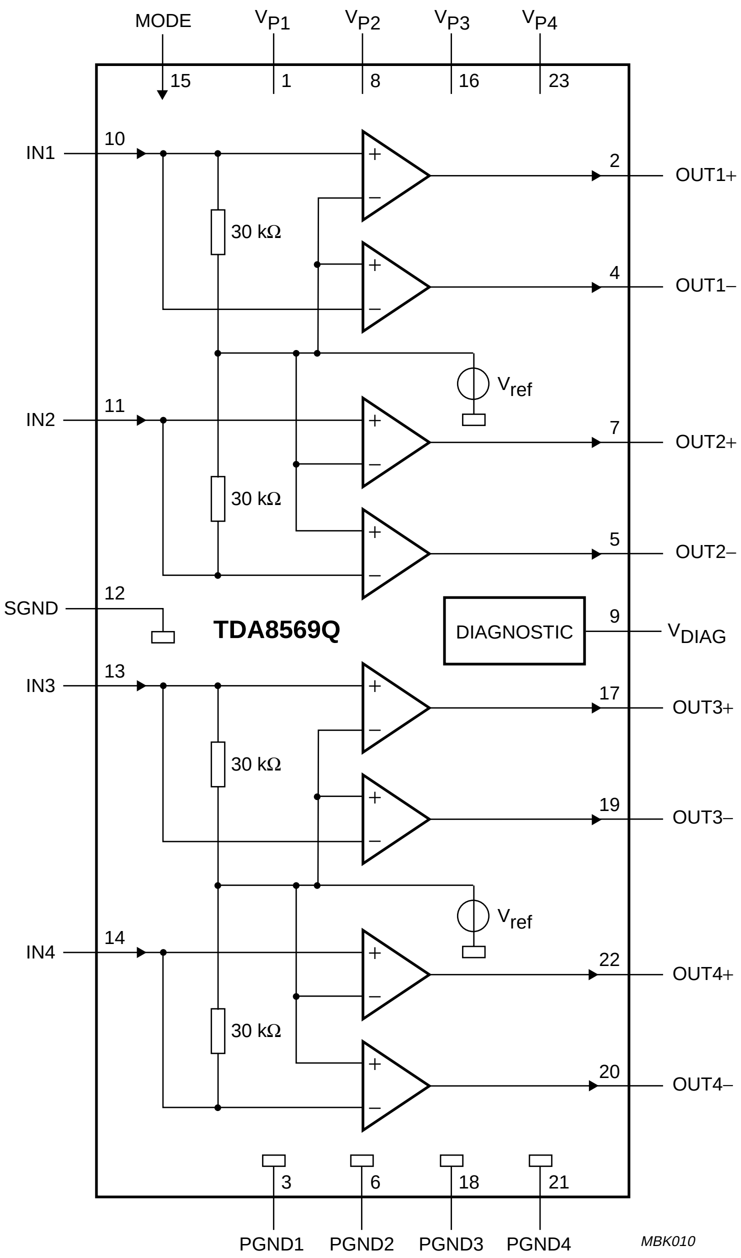


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P1}	1	supply voltage 1
OUT1+	2	output 1+
PGND1	3	power ground 1
OUT1–	4	output 1–
OUT2–	5	output 2–
PGND2	6	power ground 2
OUT2+	7	output 2+
V_{P2}	8	supply voltage 2
V_{DIAG}	9	diagnostic output
IN1	10	input 1
IN2	11	input 2
SGND	12	signal ground
IN3	13	input 3
IN4	14	input 4
MODE	15	mode select switch input
V_{P3}	16	supply voltage 3
OUT3+	17	output 3+
PGND3	18	power ground 3
OUT3–	19	output 3–
OUT4–	20	output 4–
PGND4	21	power ground 4
OUT4+	22	output 4+
V_{P4}	23	supply voltage 4

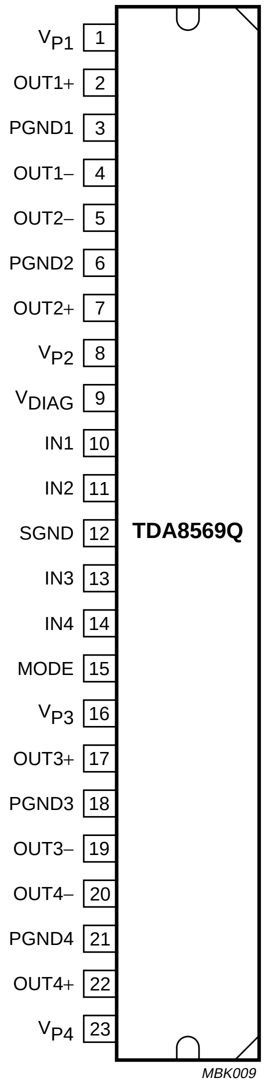


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8569Q contains four identical amplifiers which can be used for bridge applications. The gain of each amplifier is fixed at 26 dB.

Mode select switch (pin MODE)

- Standby: low supply current (<100 μA)
- Mute: input signal suppressed
- Operating: normal on condition.

Since this pin has a low input current (<80 μA), a low cost supply switch can be applied.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥150 ms (charging of the input capacitors at pins IN1, IN2, IN3 and IN4).

This can be realized by:

- Microprocessor control
- External timing circuit (see Fig.3).

Diagnostic output (pin V_{DIAG})

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin V_{DIAG} goes LOW. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and so limit the distortion. The output level of pin V_{DIAG} is independent of the number of channels that are clipping (see Fig.4).

SHORT-CIRCUIT DIAGNOSTIC

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 10 ms after removal of the short-circuit. During this short-circuit condition, pin V_{DIAG} is continuously LOW.

When a short-circuit occurs across the load of one or more channels, the output stages are switched off for approximately 10 ms. After that time it is checked during approximately 50 μs to determine whether the short-circuit is still present. Due to this duty cycle of 50 μs/10 ms the average current consumption during this short-circuit condition is very low.

During this short-circuit condition, pin V_{DIAG} is LOW for 10 ms and HIGH for 50 μs (see Fig.5). The protection circuits of all channels are coupled. This means that if a short-circuit condition occurs in **one** of the channels, **all** channels are switched off. Consequently, the power dissipation in any short-circuit condition is very low.

TEMPERATURE PRE-WARNING

When the virtual junction temperature T_{vj} reaches 145 °C, pin V_{DIAG} goes LOW.

OPEN COLLECTOR OUTPUTS

The diagnostic pin has an open-collector output, so more devices can be tied together. An external pull-up resistor is needed.

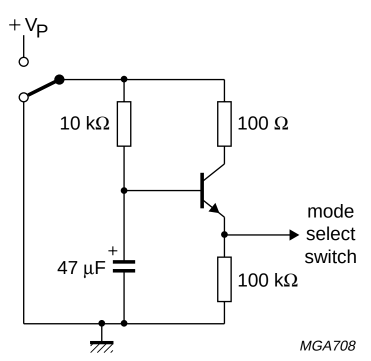


Fig.3 Mode select switch circuitry.

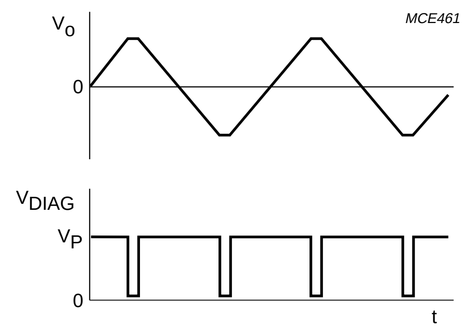


Fig.4 Distortion detector waveform.

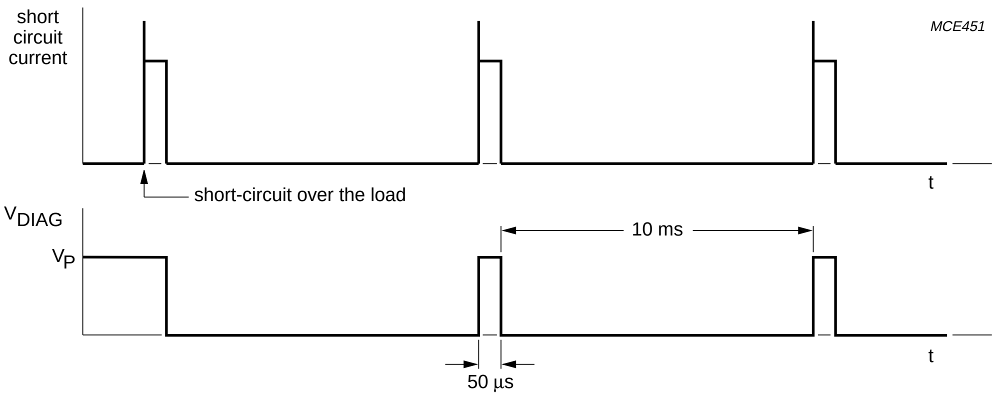


Fig.5 Short-circuit waveform.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump protection; during 50 ms; $t_r \geq 2.5$ ms	–	45	V
$V_{sc(safe)}$	short-circuit safe voltage		–	18	V
V_{rp}	reverse polarity voltage		–	6	V
I_{OSM}	non-repetitive peak output current		–	10	A
I_{ORM}	repetitive peak output current		–	7.5	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case (see Fig.6)	1	K/W

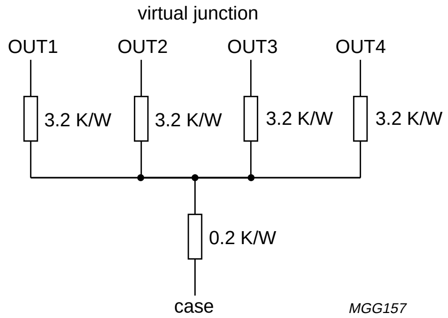


Fig.6 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6	14.4	18	V
$I_{q(tot)}$	total quiescent current	$R_L = \infty$	–	230	360	mA
Operating condition						
V_{MODE}	mode select switch level		8.5	–	V_P	V
I_{MODE}	mode select switch current	V_{MODE} = 14.4 V	–	30	80	μA
V_O	output voltage	note 2	–	7.0	–	V
V_{OS}	output offset voltage		–	–	150	mV
Mute condition						
V_{MODE}	mode select switch level		3.3	–	6.4	V
V_O	output voltage	note 2	–	7.0	–	V
V_{OS}	output offset voltage		–	–	100	mV
ΔV_{OS}	change of output offset voltage	switching between mute and operating	–	–	100	mV
Standby condition						
V_{MODE}	mode select switch level		0	–	2	V
I_{stb}	standby current		–	0.2	10	μA
Diagnostic						
V_{DIAG}	diagnostic output voltage	during any fault condition	–	–	0.6	V
T_{vj}	temperature pre-warning	V_{DIAG} = 0.6 V	–	145	–	°C

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At V_P = 18 to 30 V the DC output voltage ≤ $\frac{1}{2}V_P$.

AC CHARACTERISTICS

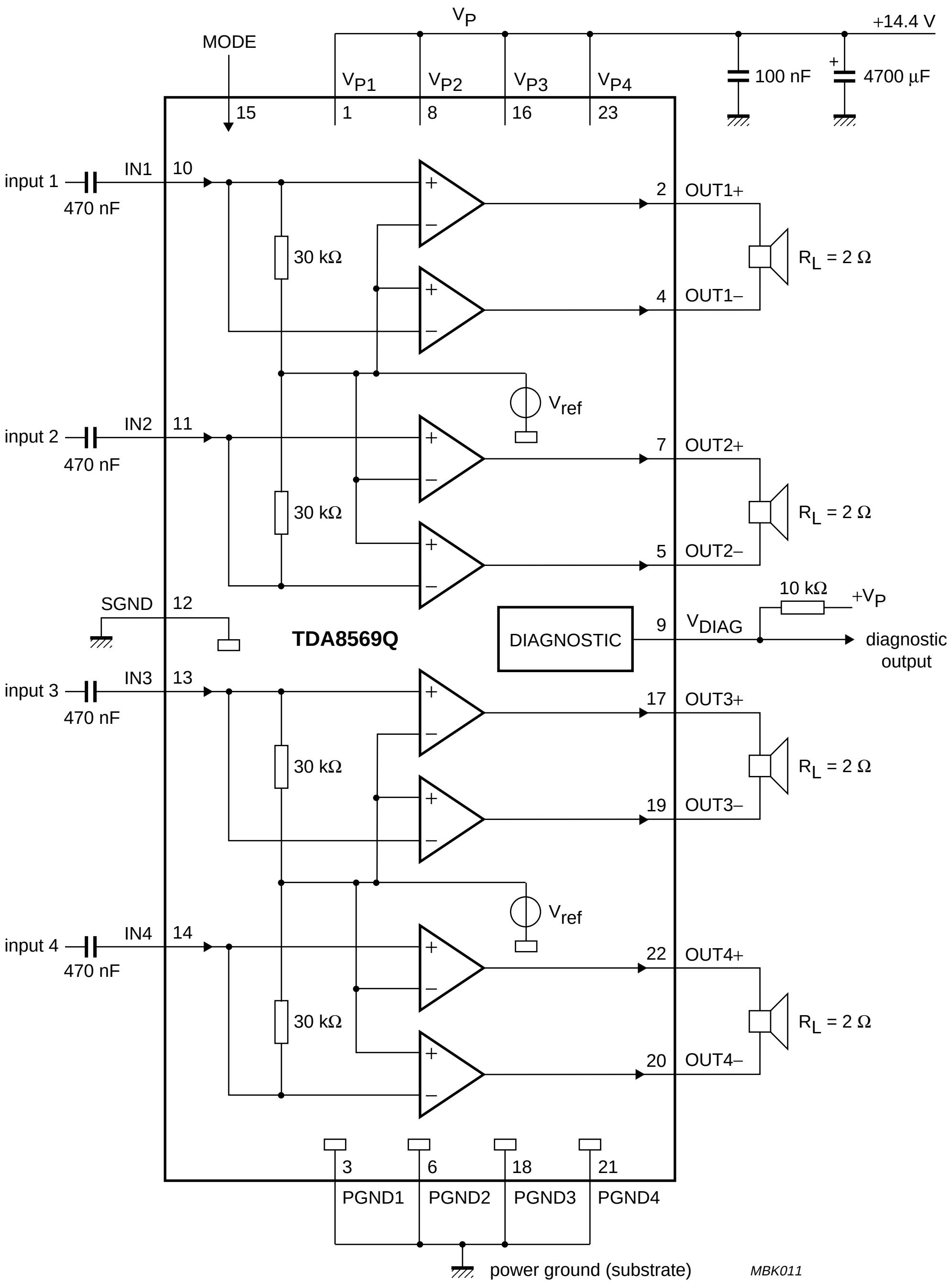
V_P = 14.4 V; R_L = 2 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in the circuit of Fig.7; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%	25	30	–	W
		THD = 10%	33	40	–	W
		V_P = 13.2 V; THD = 0.5%	–	25	–	W
		V_P = 13.2 V; THD = 10%	–	35	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
		V_{DIAG} ≤ 0.6 V; note 1	–	10	–	%
B_p	power bandwidth	THD = 0.5%; P_o = –1 dB with respect to 16 W	–	20 to 20000	–	Hz
$f_{ro(l)}$	low frequency roll-off	at –1 dB; note 2	–	25	–	Hz
$f_{ro(h)}$	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	on; note 3	50	60	–	dB
		mute; note 3	50	60	–	dB
		standby; note 3	80	90	–	dB
$\|Z_i\|$	input impedance		25	30	38	kΩ
$V_{n(o)}$	noise output voltage	on; note 4	–	85	120	μV
		on; note 5	–	100	–	μV
		mute; note 6	–	60	–	μV
α_{cs}	channel separation	note 7	45	55	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
V_o	output signal in mute	note 8	–	–	2	mV
P_o	output power	THD = 0.5%; R_L = 4 Ω	–	19	–	W
		THD = 10%; R_L = 4 Ω	–	25	–	W
$P_{o(EIAJ)}$	EIAJ output power	THD = maximum; square wave input; V_i = 2 V (p-p)	–	40	–	W
THD	total harmonic distortion	P_o = 1 W; R_L = 4 Ω	–	0.05	–	%

Notes

1. Dynamic Distortion Detector (DDD) active, pin V_{DIAG} is set to logic 0.
2. Frequency response externally fixed.
3. V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.
4. B = 20 Hz to 20 kHz; R_s = 0 Ω.
5. B = 20 Hz to 20 kHz; R_s = 10 kΩ.
6. B = 20 Hz to 20 kHz; independent of R_s.
7. P_o = 25 W; R_s = 10 kΩ.
8. V_i = $V_{i(max)}$ = 1 V (RMS).

TEST AND APPLICATION INFORMATION



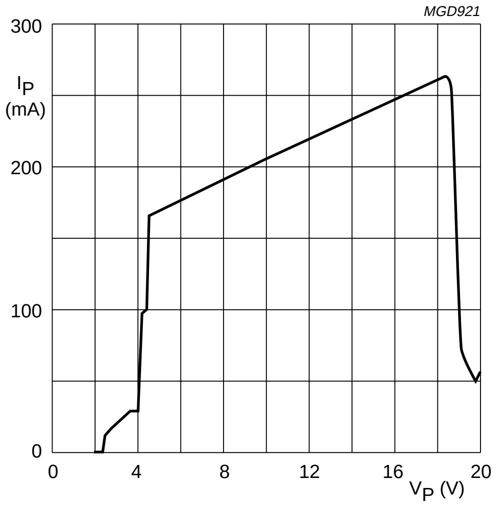
Special care must be taken in the PCB-layout to separate pin V_{DIAG} from the pins IN1, IN2, IN3 and IN4 to minimize the crosstalk between the clip output and the inputs.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode for a period of ≥150 ms (charging the input capacitors at pins IN1, IN2, IN3 and IN4).

Fig.7 Application circuit diagram.

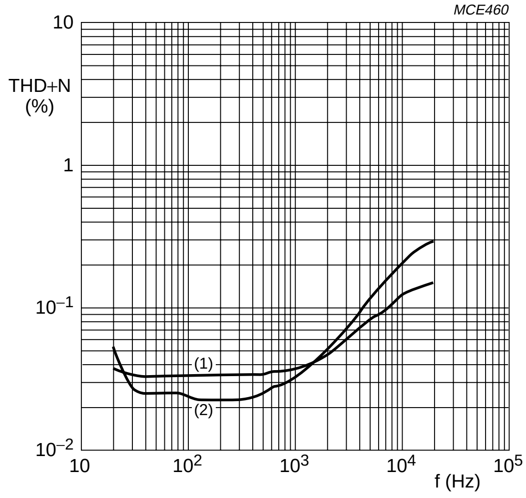
Test information

Figures 8 to 15 have the following conditions: V_P = 14.4 V; f = 1 kHz; 80 kHz filter used; unless otherwise specified.



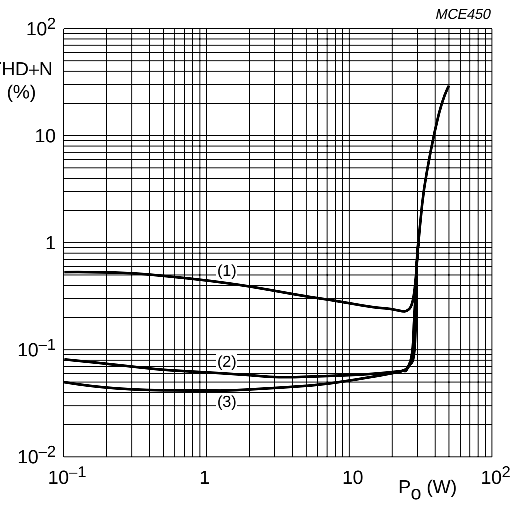
$R_L = \infty$.

Fig.8 I_P as a function of V_P.



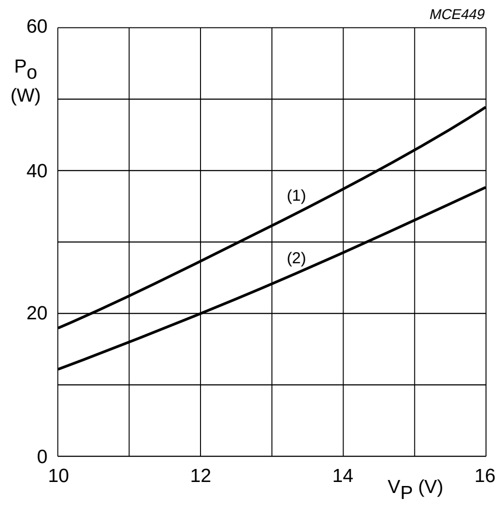
$R_L = 2\ \Omega$.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.9 THD + N as a function of frequency.



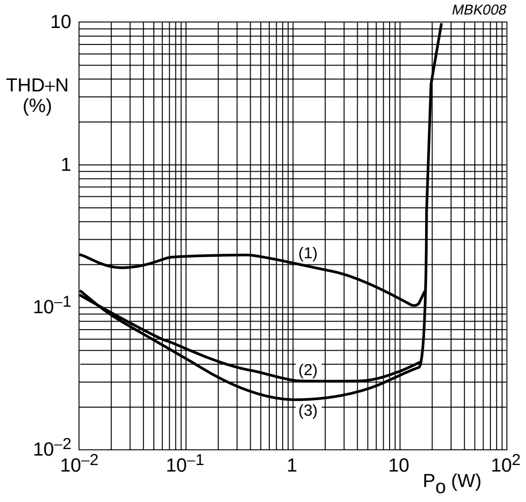
$R_L = 2\ \Omega$.
(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.10 THD + N as a function of P_o.



$R_L = 2\ \Omega$.
(1) THD = 10%.
(2) THD = 0.5%.

Fig.11 P_o as a function of V_P.



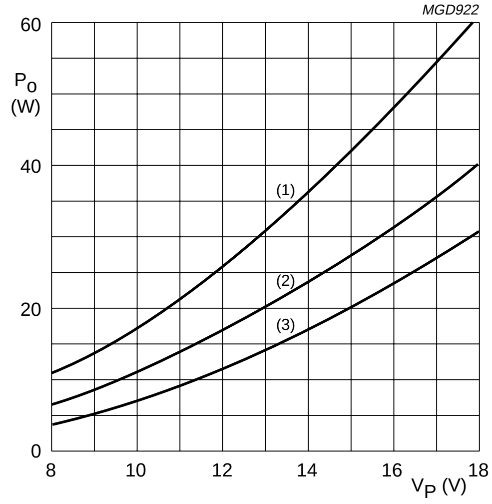
$R_L = 4\ \Omega$.

(1) f = 10 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

Fig.12 THD + N as a function of P_o.



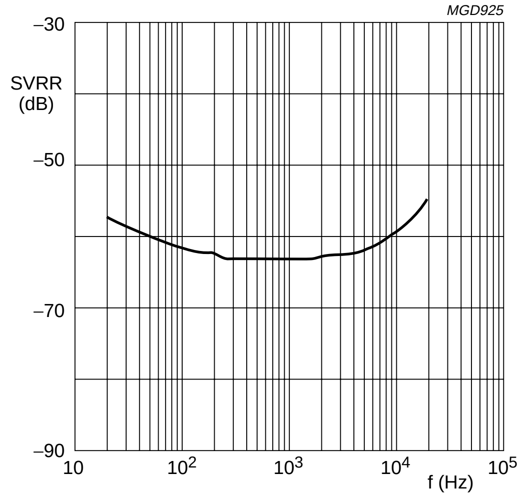
$R_L = 4\ \Omega$.

(1) EIAJ.

(2) THD = 10%.

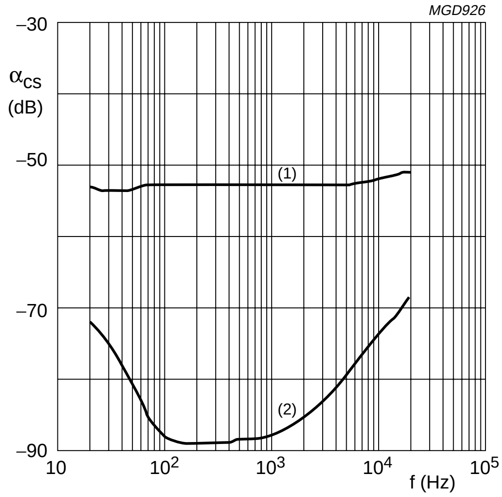
(3) THD = 0.5%.

Fig.13 P_o as a function of V_P.



$R_L = 4\ \Omega$.

Fig.14 SVRR as a function of frequency.



$R_L = 4\ \Omega$.

(1) channel 1 ⇔ channel 2, channel 3 ⇔ channel 4.

(2) channels 1 and 2 ⇔ channels 3 and 4.

Fig.15 Channel separation as a function of frequency.

PCB layout

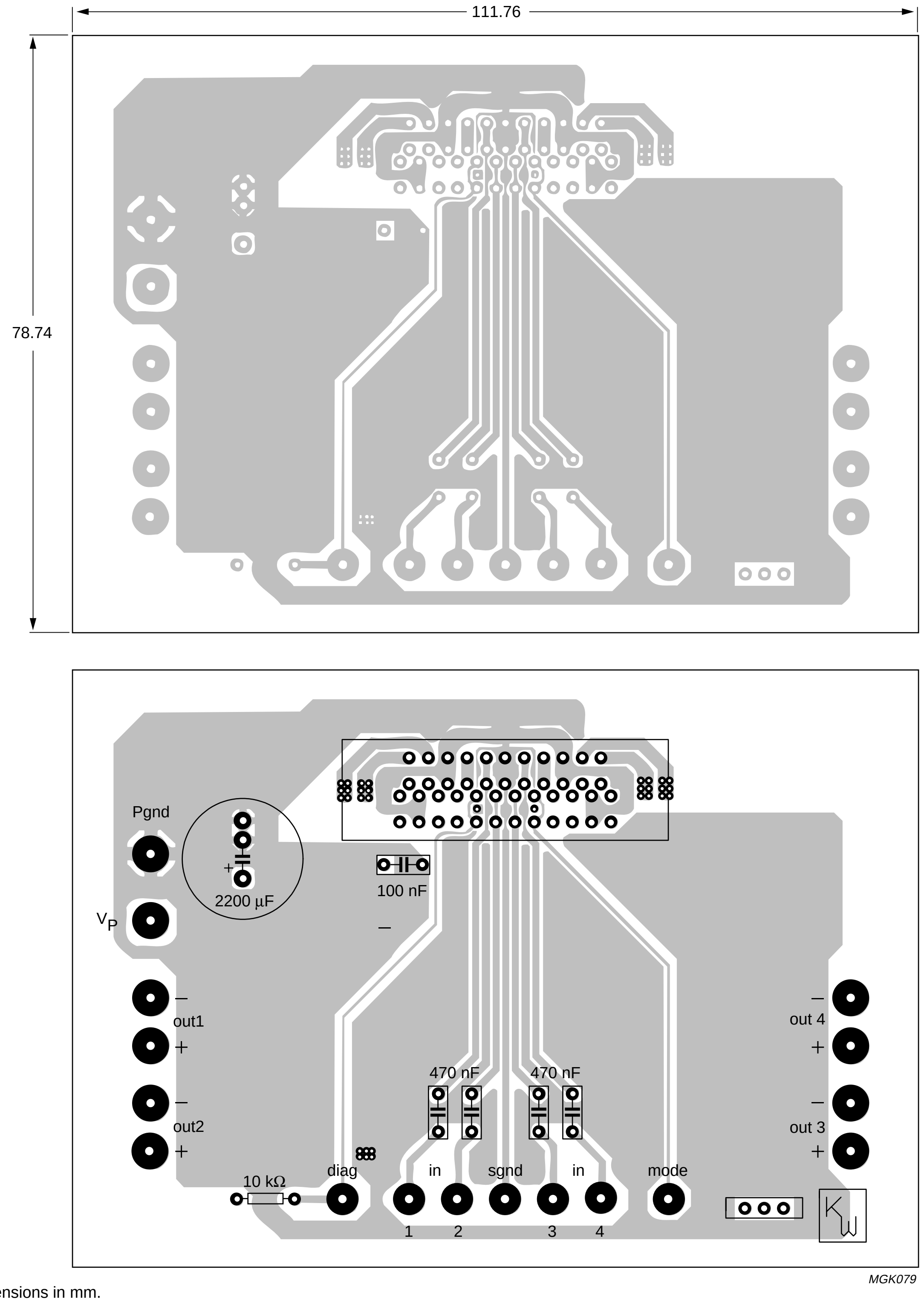
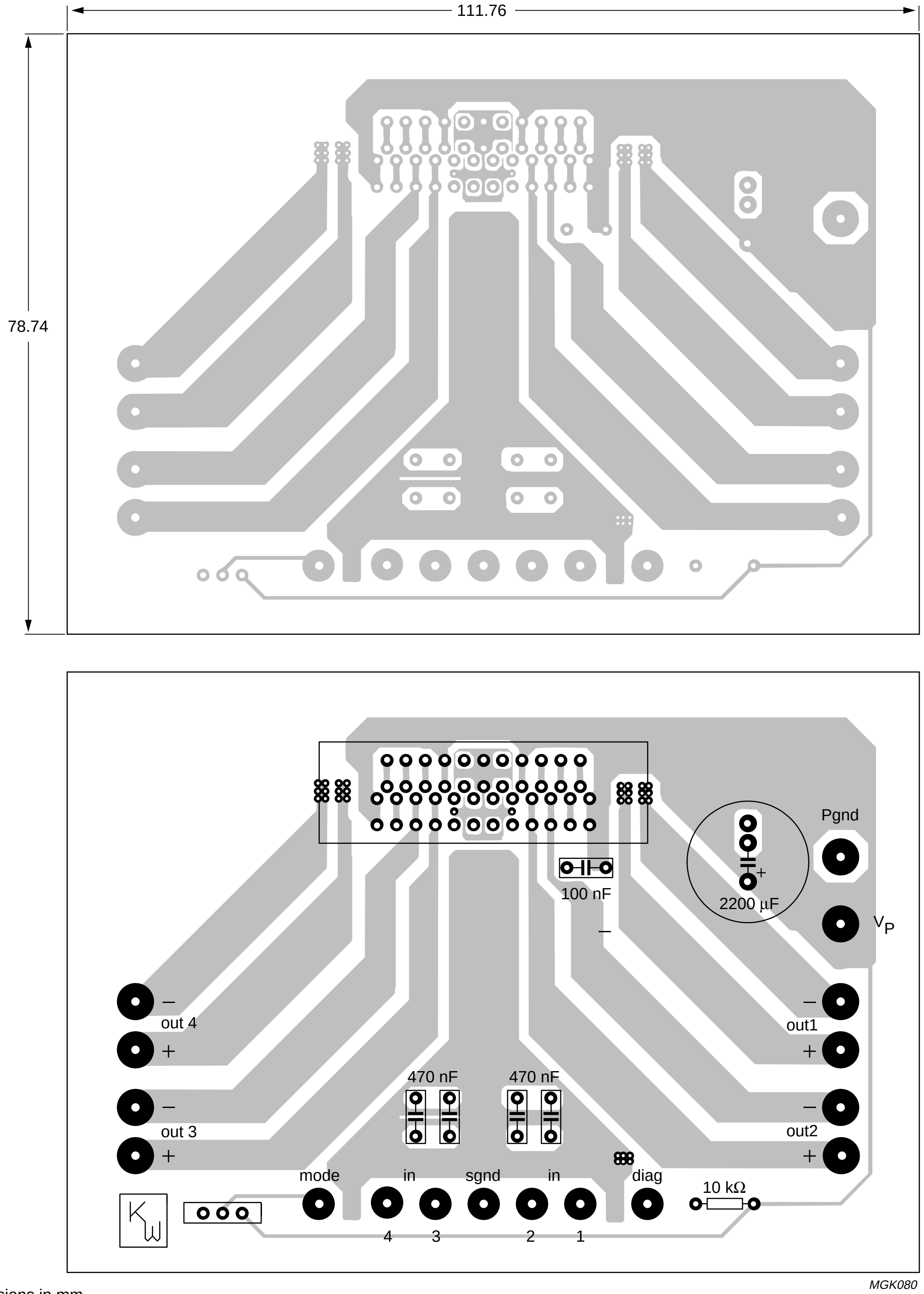


Fig.16 PCB layout (component side).

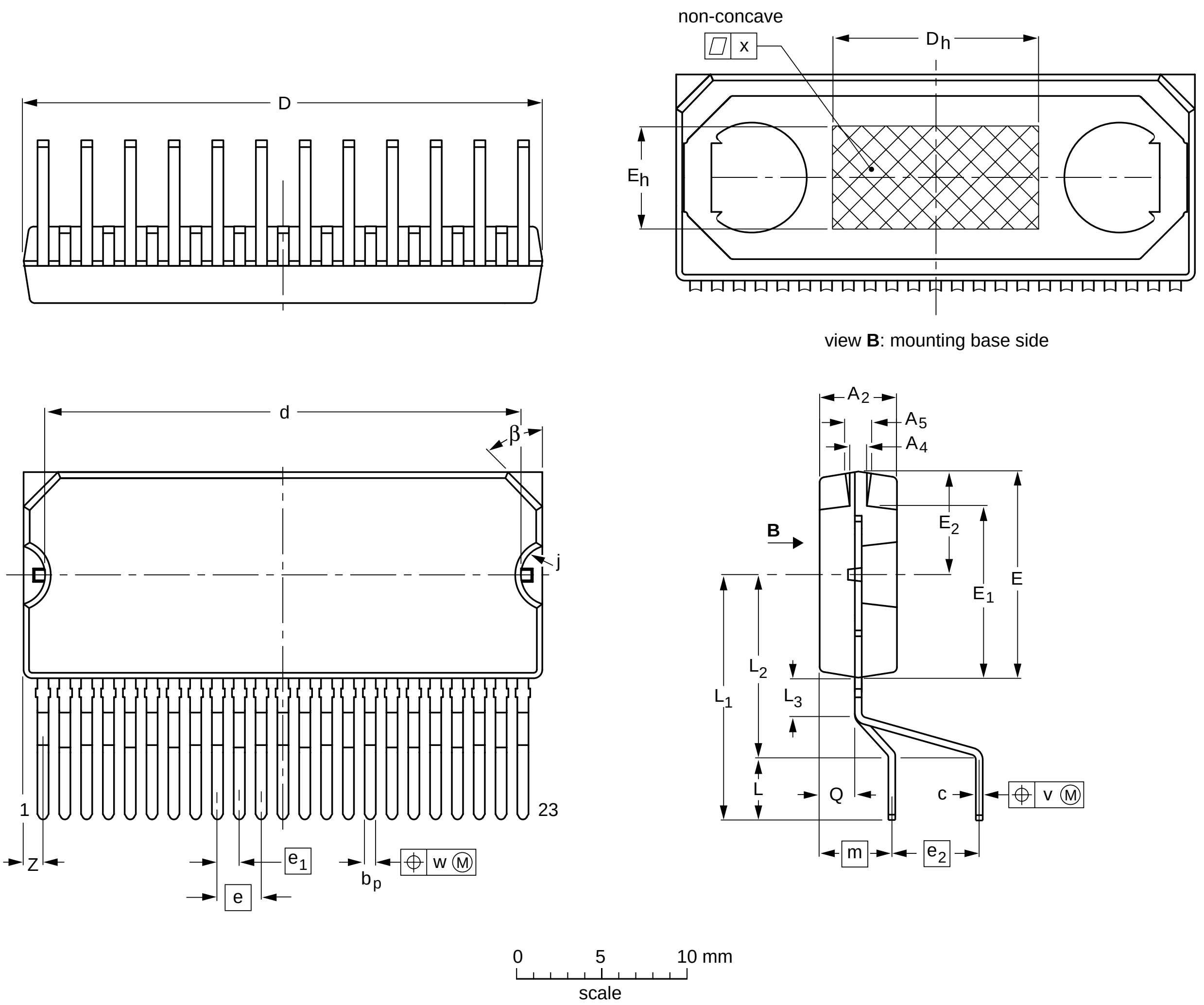


Dimensions in mm.

Fig.17 PCB layout (soldering side).

PACKAGE OUTLINE

DBS23P: plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm) **SOT411-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	E_2	j	L	L_1	L_2	L_3	m	Q	v	w	x	β	$Z^{(1)}$
mm	4.6 4.3	1.15 0.85	1.65 1.35	0.75 0.60	0.55 0.35	30.4 29.9	28.0 27.5	12	12.2 11.8	2.54	1.27	5.08	6	10.15 9.85	6.2 5.8	1.85 1.65	3.6 2.8	14 13	10.7 9.9	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	45°	1.43 0.78

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT411-1						~~98-02-20~~ 02-04-24

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable(1)

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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