

# 18-Mbit (512K × 36/1M × 18) Pipelined DCD Sync SRAM

## Features

- Supports bus operation up to 200 MHz
- Available speed grades are 200, and 167 MHz
- Registered inputs and outputs for pipelined operation
- Optimal for performance (double-cycle deselect)
- Depth expansion without wait state
- 3.3 V core power supply ( $V_{DD}$ )
- 2.5 V or 3.3 V I/O power supply ( $V_{DDQ}$ )
- Fast clock-to-output times
  - 3 ns (for 200 MHz device)
- Provides high performance 3-1-1-1 access rate
- User selectable burst counter supporting interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed writes
- Asynchronous output enable
- CY7C1386KV33 available in JEDEC-standard Pb-free 100-pin TQFP. CY7C1387KV33 available in JEDEC-standard Pb-free 100-pin TQFP
- ZZ sleep mode option

## Functional Description

The CY7C1386KV33/CY7C1387KV33 SRAM integrates 512K × 36/1M × 18 SRAM cells with advanced synchronous peripheral circuitry and a two-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive edge triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ( $\overline{CE}_1$ ), depth expansion chip enables ( $\overline{CE}_2$  and  $\overline{CE}_3$ ), burst control inputs ( $\overline{ADSC}$ ,  $\overline{ADSP}$ , and  $\overline{ADV}$ ), write enables ( $\overline{BW}_X$ , and  $\overline{BWE}$ ), and global write ( $\overline{GW}$ ). Asynchronous inputs include the output enable ( $\overline{OE}$ ) and the ZZ pin.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor ( $\overline{ADSP}$ ) or address strobe controller ( $\overline{ADSC}$ ) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ( $\overline{ADV}$ ).

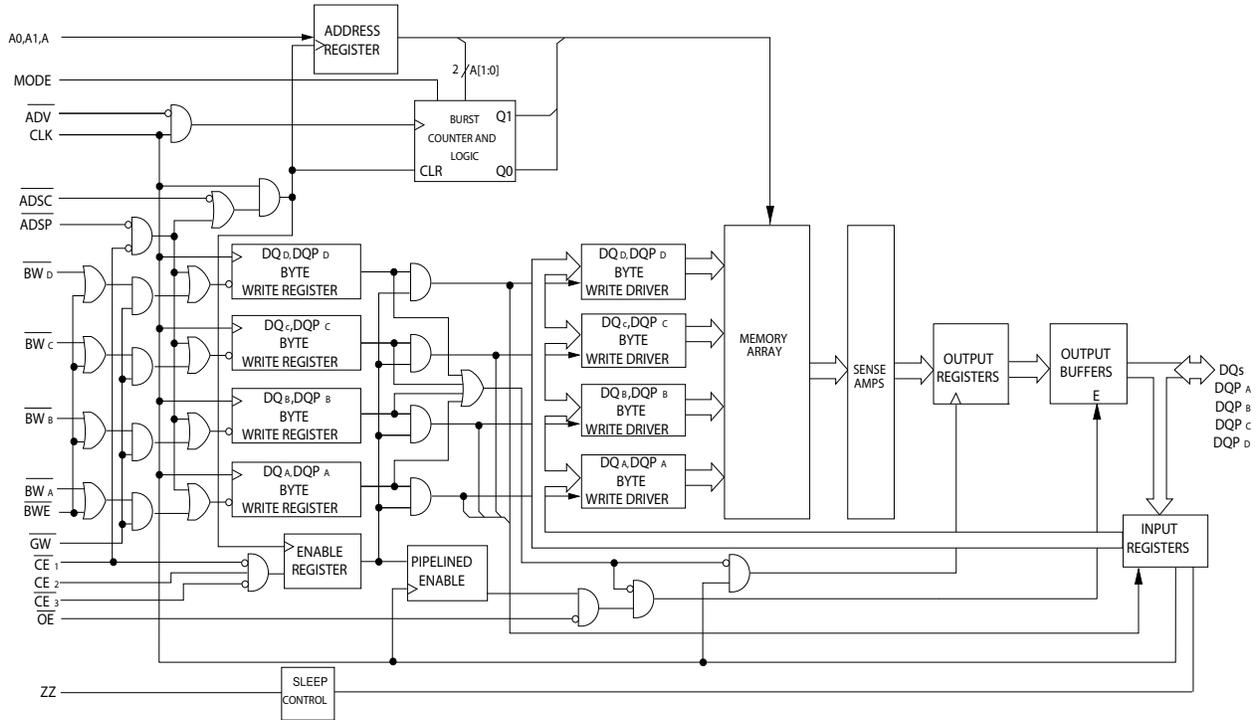
Address, data inputs, and write controls are registered on-chip to initiate a self timed write cycle. This part supports byte write operations (see [Pin Configurations on page 5](#) and [Truth Table on page 9](#) for further details). Write cycles can be one to four bytes wide as controlled by the byte write control inputs.  $\overline{GW}$  active LOW causes all bytes to be written. This device incorporates an additional pipelined enable register which delays turning off the output buffers an additional cycle when a deselect is executed. This feature allows depth expansion without penalizing system performance.

The CY7C1386KV33/CY7C1387KV33 operates from a +3.3 V core power supply while all outputs operate with a +3.3 V or +2.5 V supply. All inputs and outputs are JEDEC-standard and JESD8-5-compatible.

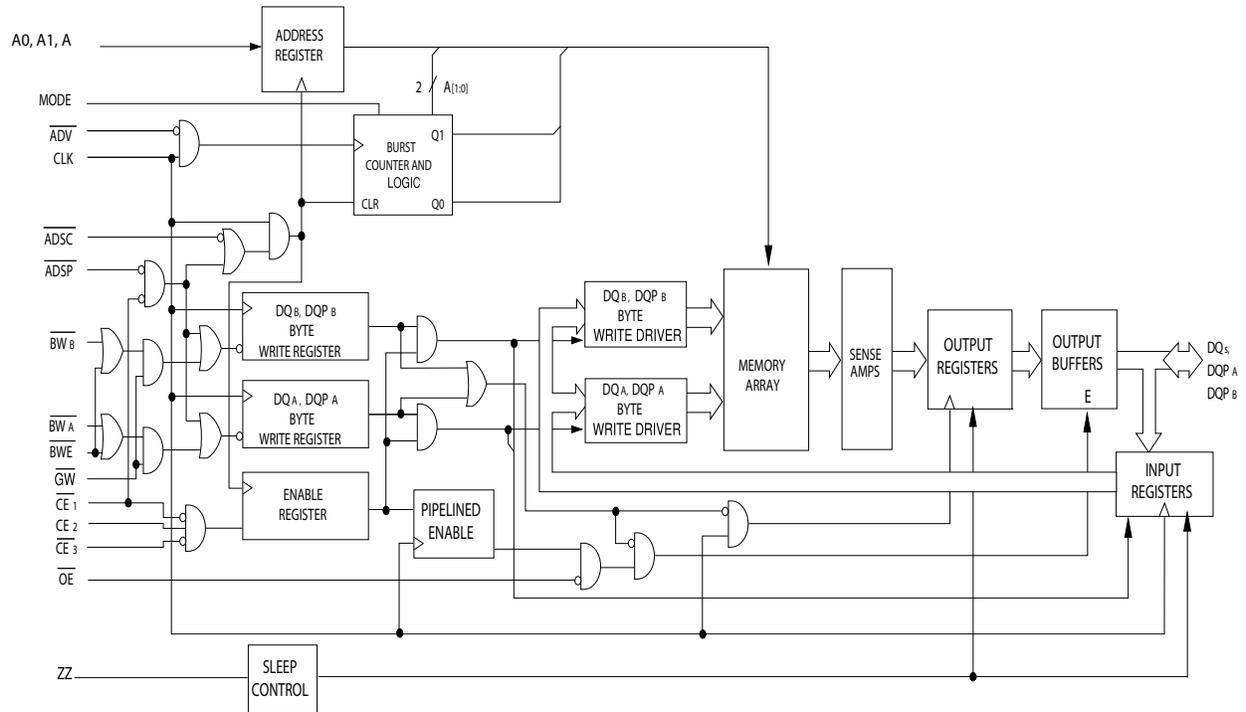
## Selection Guide

Description		200 MHz	167 MHz	Unit
Maximum access time		3.0	3.4	ns
Maximum operating current	× 18	158	143	mA
	× 36	178	163	

**Logic Block Diagram – CY7C1386KV33**



**Logic Block Diagram – CY7C1387KV33**

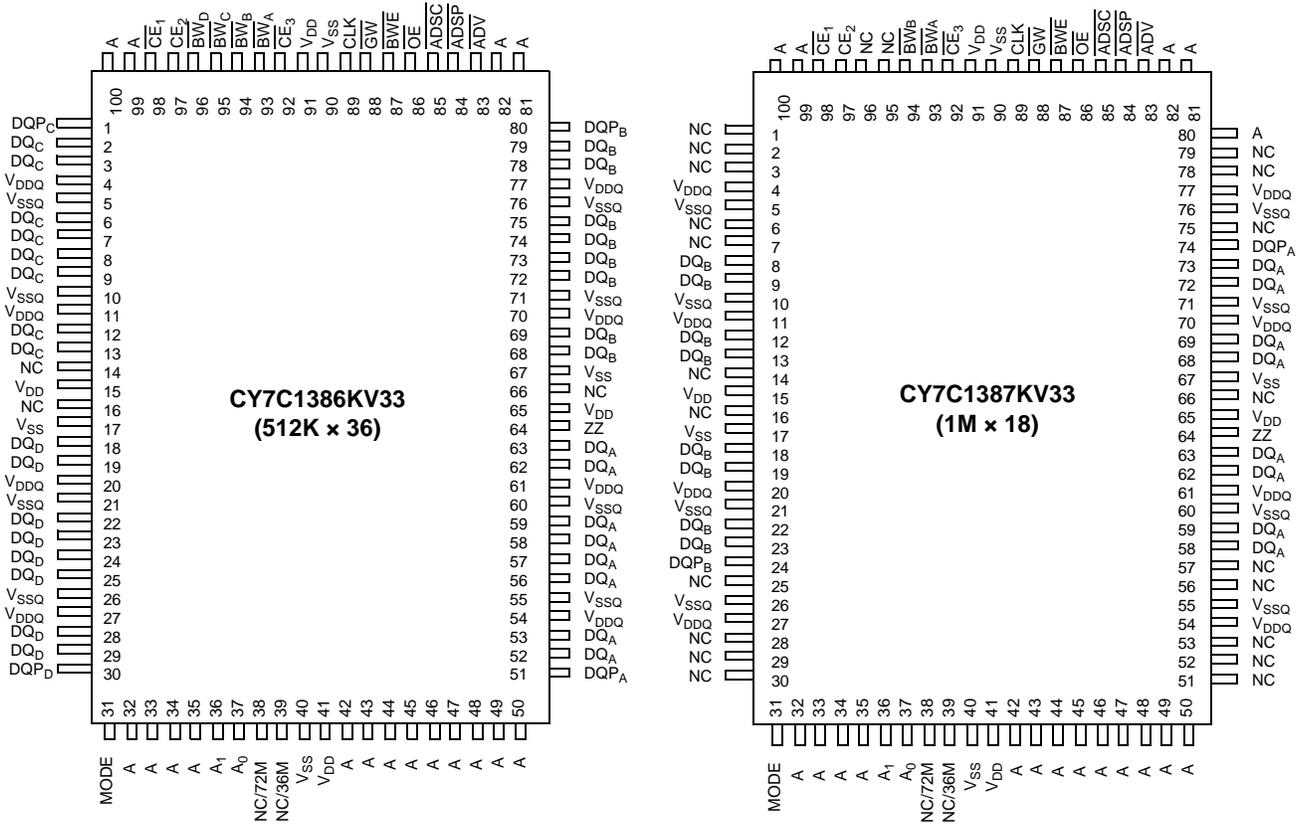


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### Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (3 Chip Enable)



## Pin Definitions

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-Synchronous	<b>Address inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and $\overline{CE}_1$ , $\overline{CE}_2$ , and $\overline{CE}_3$ are sampled active. A1:A0 are fed to the two-bit counter.
$\overline{BW}_A$ , $\overline{BW}_B$ , $\overline{BW}_C$ , $\overline{BW}_D$	Input-Synchronous	<b>Byte write select inputs, active LOW.</b> Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	<b>Global write enable input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_X$ and $\overline{BWE}$ ).
$\overline{BWE}$	Input-Synchronous	<b>Byte write enable input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	<b>Clock input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-Synchronous	<b>Chip enable 1 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_2$ and $\overline{CE}_3$ to select or deselect the device. ADSP is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
$\overline{CE}_2$	Input-Synchronous	<b>Chip enable 2 input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. $\overline{CE}_2$ is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-Synchronous	<b>Chip enable 3 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_2$ to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input-Asynchronous	<b>Output enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, DQ pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-Synchronous	<b>Advance input signal, sampled on the rising edge of CLK, active LOW.</b> When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-Synchronous	<b>Address strobe from processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when $\overline{CE}_1$ is deasserted HIGH.
ADSC	Input-Synchronous	<b>Address strobe from controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A1:A0 are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ	Input-Asynchronous	<b>ZZ sleep input, active HIGH.</b> When asserted HIGH places the device in a non-time critical sleep condition with data integrity preserved. For normal operation, this pin has to be LOW. ZZ pin has an internal pull down.
DQs, DQP <sub>X</sub>	I/O-Synchronous	<b>Bidirectional data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQs and DQP <sub>X</sub> are placed in a tristate condition.
V <sub>DD</sub>	Power Supply	<b>Power supply inputs to the core of the device.</b>
V <sub>SS</sub>	Ground	<b>Ground for the core of the device.</b>
V <sub>SSQ</sub>	I/O Ground	<b>Ground for the I/O circuitry.</b>
V <sub>DDQ</sub>	I/O Power Supply	<b>Power supply for the I/O circuitry.</b>

## Pin Definitions (continued)

Name	I/O	Description
MODE	Input-Static	<b>Selects burst order.</b> When tied to GND selects linear burst sequence. When tied to $V_{DD}$ or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull up.
NC	–	<b>No Connects.</b> Not internally connected to the die.
NC/(36 M, 72 M, 144 M, 288 M, 576 M, 1 G)	–	<b>These pins are not connected.</b> They are used for expansion up to 36M, 72M, 144M, 288M, 576M, and 1G densities.

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock.

The CY7C1386KV33/CY7C1387KV33 supports secondary cache in systems using either a linear or interleaved burst sequence. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ( $\overline{ADSP}$ ) or the controller address strobe ( $\overline{ADSC}$ ). Address advancement through the burst sequence is controlled by the  $\overline{ADV}$  input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ( $\overline{BWE}$ ) and byte write select ( $\overline{BW}_X$ ) inputs. A global write enable ( $\overline{GW}$ ) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Synchronous chip selects  $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$  and an asynchronous output enable ( $\overline{OE}$ ) provide for easy bank selection and output tristate control.  $\overline{ADSP}$  is ignored if  $\overline{CE}_1$  is HIGH.

### Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{ADSP}$  or  $\overline{ADSC}$  is asserted LOW, (2) chip selects are all asserted active, and (3) the write signals ( $\overline{GW}$ ,  $\overline{BWE}$ ) are all deasserted HIGH.  $\overline{ADSP}$  is ignored if  $\overline{CE}_1$  is HIGH. The address presented to the address inputs is stored into the address advancement logic and the address register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the output registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within  $t_{CO}$  if  $\overline{OE}$  is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always tristated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the  $\overline{OE}$  signal. Consecutive single read cycles are supported.

The CY7C1386KV33/CY7C1387KV33 is a double cycle deselect part. After the SRAM is deselected at clock rise by the chip select and either  $\overline{ADSP}$  or  $\overline{ADSC}$  signals, its output tristates immediately after the next clock rise.

### Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1)  $\overline{ADSP}$  is asserted LOW and (2) chip select is asserted active. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The write signals ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW}_X$ ) and  $\overline{ADV}$  inputs are ignored during this first cycle.

$\overline{ADSP}$  triggered write accesses require two clock cycles to complete. If  $\overline{GW}$  is asserted LOW on the second clock rise, the data presented to the  $DQ_X$  inputs is written into the corresponding address location in the memory core. If  $\overline{GW}$  is HIGH, the write operation is controlled by  $\overline{BWE}$  and  $\overline{BW}_X$  signals.

The CY7C1386KV33/CY7C1387KV33 provides byte write capability that is described in the write cycle description table. Asserting the byte write enable input ( $\overline{BWE}$ ) with the selected byte write input, selectively writes to the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations.

The CY7C1386KV33/CY7C1387KV33 is a common I/O device, the output enable ( $\overline{OE}$ ) must be deasserted HIGH before presenting data to the  $DQ$  inputs. This tristates the output drivers. As a safety precaution,  $DQ$  are automatically tristated whenever a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$  write accesses are initiated when the following conditions are satisfied: (1)  $\overline{ADSC}$  is asserted LOW, (2)  $\overline{ADSP}$  is deasserted HIGH, (3) chip select is asserted active, and (4) the appropriate combination of the write inputs ( $\overline{GW}$ ,  $\overline{BWE}$ , and  $\overline{BW}_X$ ) are asserted active to conduct a write to the desired byte(s).  $\overline{ADSC}$  triggered write accesses require a single clock cycle to complete. The address presented is loaded into the address register and the address advancement logic while being delivered to the memory core. The  $\overline{ADV}$  input is ignored during this cycle. If a global write is conducted, the data presented to the  $DQ_X$  is

written into the corresponding address location in the memory core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations.

The CY7C1386KV33/CY7C1387KV33 is a common I/O device, the output enable ( $\overline{OE}$ ) must be deasserted HIGH before presenting data to the  $DQ_X$  inputs. This tristates the output drivers. As a safety precaution,  $DQ_X$  are automatically tristated whenever a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Burst Sequences

The CY7C1386KV33/CY7C1387KV33 provides a two-bit wraparound counter, fed by  $A_{[1:0]}$ , that implements either an interleaved or linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting  $\overline{ADV}$  LOW at clock rise automatically increments the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be

deselected prior to entering the sleep mode.  $\overline{CEs}$ ,  $\overline{ADSP}$ , and  $\overline{ADSC}$  must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

### Interleaved Burst Address Table

(MODE = Floating or  $V_{DD}$ )

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

## ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	65	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
$t_{ZZI}$	ZZ Active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
$t_{RZZI}$	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

## Truth Table

The Truth Table for CY7C1386KV33 and CY7C1387KV33 follow. [1, 2, 3, 4, 5]

Operation	Add. Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tristate
Deselect cycle, power-down	None	L	X	H	L	H	L	X	X	X	L-H	Tristate
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tristate
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L-H	Tristate
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L-H	Tristate
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tristate
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tristate
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tristate
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tristate
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

### Notes

1. X = Do not care, H = Logic HIGH, L = Logic LOW.
2.  $\overline{WRITE}$  = L when any one or more byte write enable signals, and  $\overline{BWE}$  = L or  $\overline{GW}$  = L.  $\overline{WRITE}$  = H when all byte write enable signals,  $\overline{BWE}$ ,  $\overline{GW}$  = H.
3. The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
4. The  $\overline{SRAM}$  always initiates a read cycle when  $\overline{ADSP}$  is asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_x$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result,  $\overline{OE}$  must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate.  $\overline{OE}$  is a don't care for the remainder of the write cycle.
5.  $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when  $\overline{OE}$  is active (LOW).

## Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1386KV33 follows. [6, 7]

Function (CY7C1386KV33)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_D$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	H	L	H	H	H	L
Write byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	H	L	H	H	L	H
Write bytes B, A	H	L	H	H	L	L
Write byte C – (DQ <sub>C</sub> and DQP <sub>C</sub> )	H	L	H	L	H	H
Write bytes C, A	H	L	H	L	H	L
Write bytes C, B	H	L	H	L	L	H
Write bytes C, B, A	H	L	H	L	L	L
Write byte D – (DQ <sub>D</sub> and DQP <sub>D</sub> )	H	L	L	H	H	H
Write bytes D, A	H	L	L	H	H	L
Write bytes D, B	H	L	L	H	L	H
Write bytes D, B, A	H	L	L	H	L	L
Write bytes D, C	H	L	L	L	H	H
Write bytes D, C, A	H	L	L	L	H	L
Write bytes D, C, B	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

## Truth Table for Read/Write

The Truth Table for Read/Write for CY7C1387KV33 follows. [6, 7]

Function (CY7C1387KV33)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}_B$	$\overline{BW}_A$
Read	H	H	X	X
Read	H	L	H	H
Write byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	H	L	H	L
Write byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	H	L	L	H
Write all bytes	H	L	L	L
Write all bytes	L	X	X	X

### Notes

6. The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.

7. Table only lists a partial listing of the byte write combinations. Any combination of  $\overline{BW}_x$  is valid appropriate write is done based on which byte write is active.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Ambient temperature with power applied .....	-55 °C to +125 °C
Supply voltage on V <sub>DD</sub> relative to GND .....	-0.5 V to +4.6 V
Supply voltage on V <sub>DDQ</sub> relative to GND .....	-0.5 V to +V <sub>DD</sub>
DC voltage applied to outputs in tristate .....	-0.5 V to V <sub>DDQ</sub> + 0.5 V
DC input voltage .....	-0.5 V to V <sub>DD</sub> + 0.5 V
Current into outputs (LOW) .....	20 mA
Static discharge voltage (per MIL-STD-883, Method 3015) .....	> 2001 V
Latch-up current .....	> 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0 °C to +70 °C	3.3 V – 5% / +10%	2.5 V – 5% to V <sub>DD</sub>

## Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU (Device without ECC)	Logical Single-Bit Upsets	25 °C	<5	5	FIT/Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/Mb
SEL	Single Event Latch up	85 °C	0	0.1	FIT/Dev

\* No LMBU or SEL events occurred during testing; this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

## Electrical Characteristics

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions	Min	Max	Unit
V <sub>DD</sub>	Power Supply Voltage		3.135	3.6	V
V <sub>DDQ</sub>	I/O Supply Voltage	for 3.3 V I/O	3.135	V <sub>DD</sub>	V
		for 2.5 V I/O	2.375	2.625	V
V <sub>OH</sub>	Output HIGH Voltage	for 3.3 V I/O, I <sub>OH</sub> = -4.0 mA	2.4	-	V
		for 2.5 V I/O, I <sub>OH</sub> = -1.0 mA	2.0	-	V
V <sub>OL</sub>	Output LOW Voltage	for 3.3 V I/O, I <sub>OL</sub> = 8.0 mA	-	0.4	V
		for 2.5 V I/O, I <sub>OL</sub> = 1.0 mA	-	0.4	V
V <sub>IH</sub>	Input HIGH Voltage <sup>[8]</sup>	for 3.3 V I/O	2.0	V <sub>DD</sub> + 0.3 V	V
		for 2.5 V I/O	1.7	V <sub>DD</sub> + 0.3 V	V
V <sub>IL</sub>	Input LOW Voltage <sup>[8]</sup>	for 3.3 V I/O	-0.3	0.8	V
		for 2.5 V I/O	-0.3	0.7	V
I <sub>X</sub>	Input Leakage Current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA
	Input Current of MODE	Input = V <sub>SS</sub>	-30	-	μA
		Input = V <sub>DD</sub>	-	5	μA
	Input Current of ZZ	Input = V <sub>SS</sub>	-5	-	μA
Input = V <sub>DD</sub>		-	30	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-5	5	μA

### Notes

- Overshoot: V<sub>IH(AC)</sub> < V<sub>DD</sub> + 1.5 V (Pulse width less than t<sub>CYC/2</sub>), undershoot: V<sub>IL(AC)</sub> > -2 V (Pulse width less than t<sub>CYC/2</sub>).
- T<sub>Power-up</sub>: Assumes a linear ramp from 0 V to V<sub>DD(min.)</sub> of at least 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

**Electrical Characteristics** (continued)

Over the Operating Range

Parameter [8, 9]	Description	Test Conditions	Min	Max	Unit		
I <sub>DD</sub>	V <sub>DD</sub> Operating Supply	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	5-ns cycle, 200 MHz	x 18	–	180	mA
				x 36	–	200	
			6-ns cycle, 167 MHz	x 18	–	158	
				x 36	–	178	
I <sub>SB1</sub>	Automatic CE Power-down Current – TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	5-ns cycle, 200 MHz	x 18	–	75	mA
				x 36	–	80	
			6-ns cycle, 167 MHz	x 18	–	75	
				x 36	–	80	
I <sub>SB2</sub>	Automatic CE Power-down Current – CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≤ 0.3 V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> – 0.3 V, f = 0	All speed grades	x 18	–	65	mA
				x 36	–	70	
I <sub>SB3</sub>	Automatic CE Power-down Current – CMOS Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≤ 0.3 V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> – 0.3 V, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	5-ns cycle, 200 MHz	x 18	–	75	mA
				x 36	–	80	
			6-ns cycle, 167 MHz	x 18	–	75	
				x 36	–	80	
I <sub>SB4</sub>	Automatic CE Power-down Current – TTL Inputs	Max. V <sub>DD</sub> , Device Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = 0	All speed grades	x 18	–	65	mA
				x 36	–	70	

## Capacitance

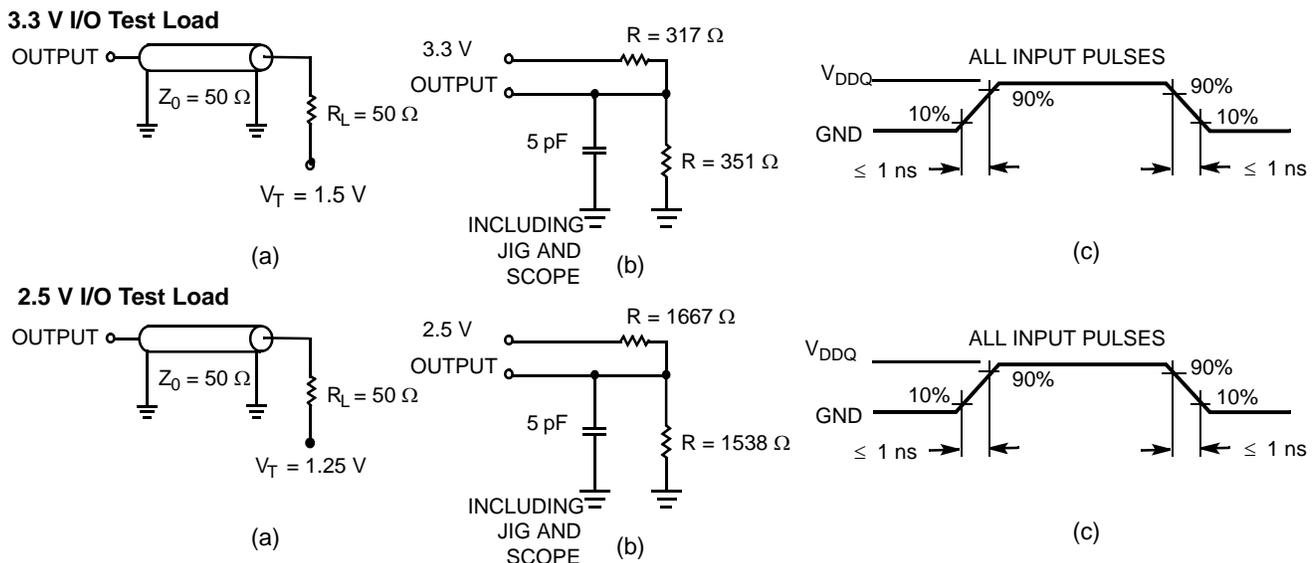
Parameter	Description	Test Conditions	100-pin TQFP Package	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{DD} = 3.3\text{ V}$ , $V_{DDQ} = 2.5\text{ V}$	5	pF
$C_{CLK}$	Clock input capacitance		5	pF
$C_{IO}$	Input/Output capacitance		5	pF

## Thermal Resistance

Parameter	Description	Test Conditions	100-pin TQFP Package	Unit	
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	With Still Air (0 m/s)	37.95	$^\circ\text{C/W}$
			With Air Flow (1 m/s)	33.19	$^\circ\text{C/W}$
			With Air Flow (3 m/s)	30.44	$^\circ\text{C/W}$
$\Theta_{JB}$	Thermal resistance (junction to board)		--	24.07	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)			8.36	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



## Switching Characteristics

Over the Operating Range

Parameter <sup>[10, 11]</sup>	Description	-200		-167		Unit
		Min	Max	Min	Max	
t <sub>POWER</sub>	V <sub>DD</sub> (typical) to the first access <sup>[12]</sup>	1	–	1	–	ms
<b>Clock</b>						
t <sub>CYC</sub>	Clock cycle time	5.0	–	6.0	–	ns
t <sub>CH</sub>	Clock HIGH	2.0	–	2.2	–	ns
t <sub>CL</sub>	Clock LOW	2.0	–	2.2	–	ns
<b>Output Times</b>						
t <sub>CO</sub>	Data output valid after CLK rise	–	3.0	–	3.4	ns
t <sub>DOH</sub>	Data output hold after CLK rise	1.3	–	1.3	–	ns
t <sub>CLZ</sub>	Clock to low Z <sup>[13, 14, 15]</sup>	1.3	–	1.3	–	ns
t <sub>CHZ</sub>	Clock to high Z <sup>[13, 14, 15]</sup>	–	3.0	–	3.4	ns
t <sub>OEV</sub>	$\overline{OE}$ LOW to output valid	–	3.0	–	3.4	ns
t <sub>OELZ</sub>	$\overline{OE}$ LOW to output low Z <sup>[13, 14, 15]</sup>	0	–	0	–	ns
t <sub>OEHZ</sub>	$\overline{OE}$ HIGH to output high Z <sup>[13, 14, 15]</sup>	–	3.0	–	3.4	ns
<b>Setup Times</b>						
t <sub>AS</sub>	Address setup before CLK rise	1.4	–	1.5	–	ns
t <sub>ADS</sub>	$\overline{ADSC}$ , $\overline{ADSP}$ setup before CLK rise	1.4	–	1.5	–	ns
t <sub>ADVS</sub>	$\overline{ADV}$ setup before CLK rise	1.4	–	1.5	–	ns
t <sub>WES</sub>	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_X$ setup before CLK rise	1.4	–	1.5	–	ns
t <sub>DS</sub>	Data input setup before CLK rise	1.4	–	1.5	–	ns
t <sub>CES</sub>	Chip enable setup before CLK rise	1.4	–	1.5	–	ns
<b>Hold Times</b>						
t <sub>AH</sub>	Address hold after CLK rise	0.4	–	0.5	–	ns
t <sub>ADH</sub>	$\overline{ADSP}$ , $\overline{ADSC}$ hold after CLK rise	0.4	–	0.5	–	ns
t <sub>ADVH</sub>	$\overline{ADV}$ hold after CLK rise	0.4	–	0.5	–	ns
t <sub>WEH</sub>	$\overline{GW}$ , $\overline{BWE}$ , $\overline{BW}_X$ hold after CLK rise	0.4	–	0.5	–	ns
t <sub>DH</sub>	Data input hold after CLK rise	0.4	–	0.5	–	ns
t <sub>CEH</sub>	Chip enable hold after CLK rise	0.4	–	0.5	–	ns

### Notes

10. Timing reference level is 1.5 V when V<sub>DDQ</sub> = 3.3 V and is 1.25 V when V<sub>DDQ</sub> = 2.5 V.

11. Test conditions shown in (a) of [Figure 2 on page 13](#) unless otherwise noted.

12. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power needs to be supplied above V<sub>DD(minimum)</sub> initially before a read or write operation can be initiated.

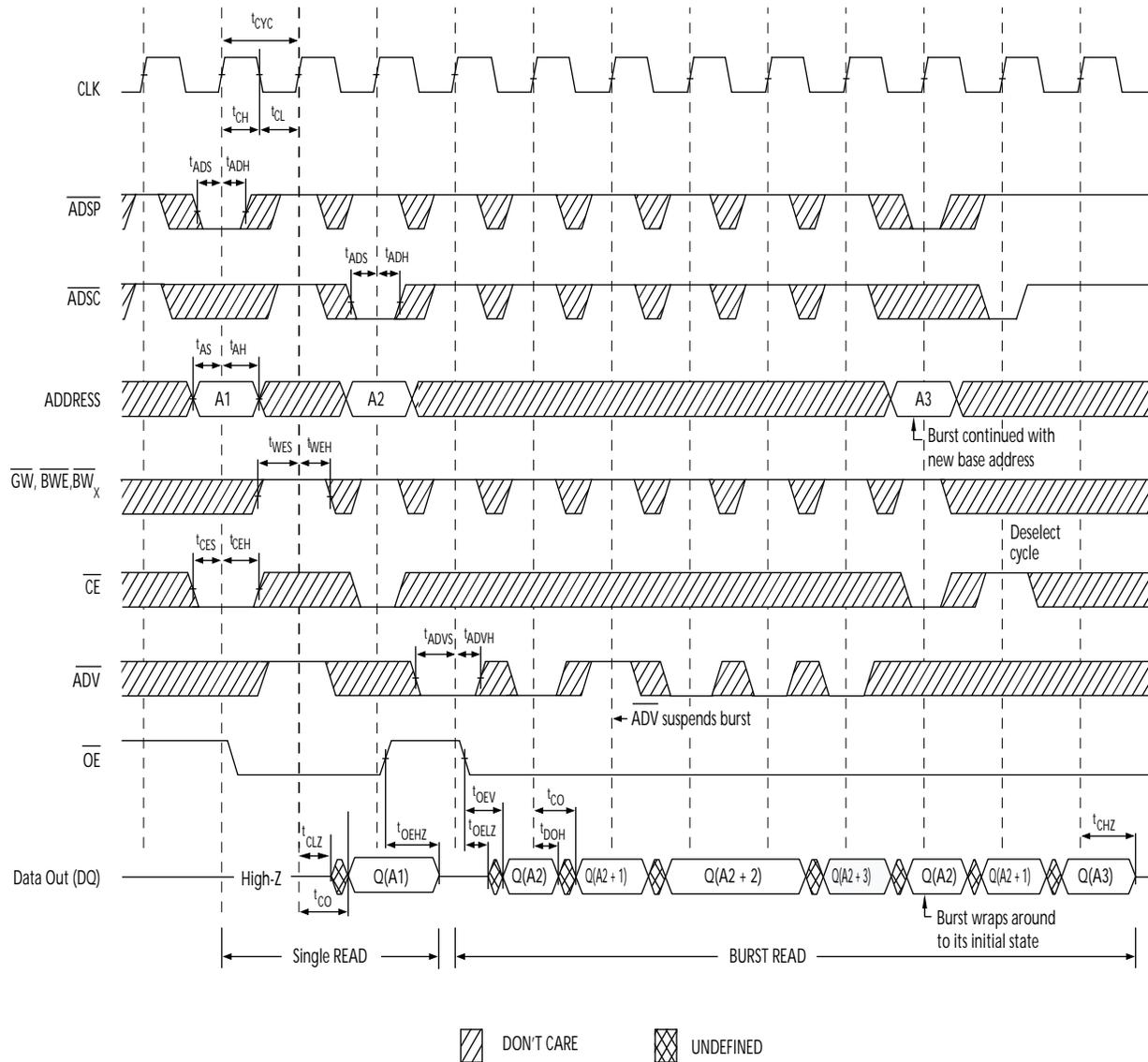
13. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OELZ</sub>, and t<sub>OEHZ</sub> are specified with AC test conditions shown in (b) of [Figure 2 on page 13](#). Transition is measured ±200 mV from steady-state voltage.

14. At any voltage and temperature, t<sub>OEHZ</sub> is less than t<sub>OELZ</sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.

15. This parameter is sampled and not 100% tested.

## Switching Waveforms

**Figure 3. Read Cycle Timing** <sup>[16]</sup>



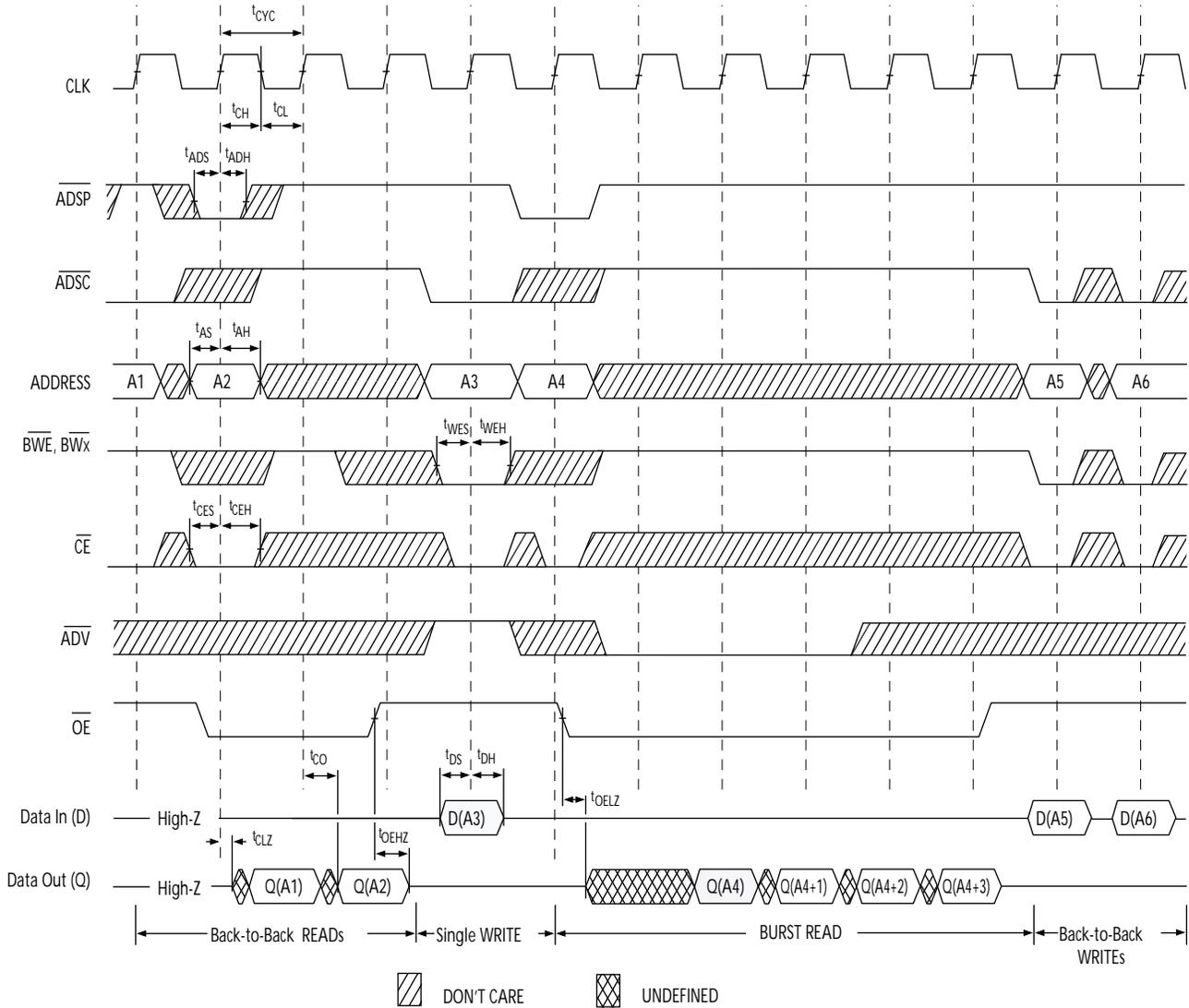
**Note**

16. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.



**Switching Waveforms** (continued)

**Figure 5. Read/Write Cycle Timing** [19, 20, 21]

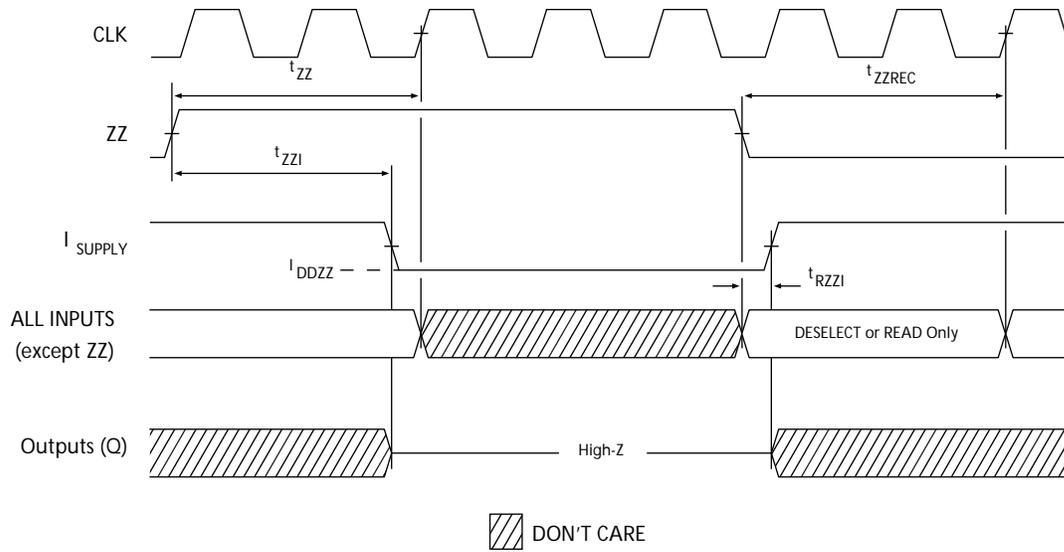


**Notes**

- 19. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.
- 20. The data bus (Q) remains in high Z following a Write cycle, unless a new read access is initiated by ADSP or ADSC.
- 21.  $\overline{GW}$  is HIGH.

**Switching Waveforms** (continued)

**Figure 6. ZZ Mode Timing** [22, 23]



**Notes**

- 22. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
- 23. DQs are in high Z when exiting ZZ sleep mode.

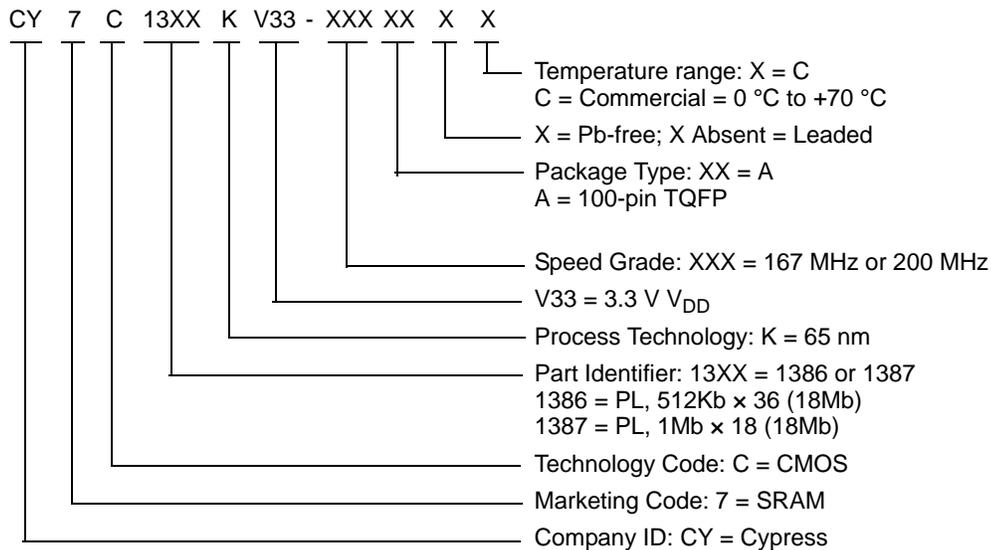
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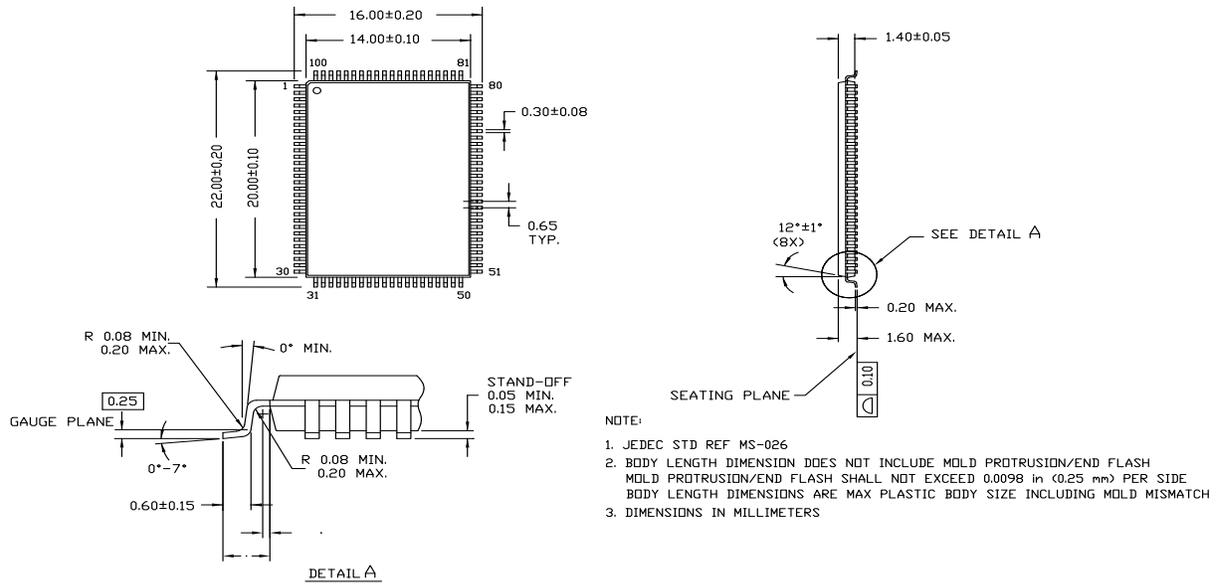
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1386KV33-167AXC	51-85050	100-pin TQFP (14 x 20 x 1.4 mm) Pb-free	Commercial
	CY7C1387KV33-167AXC			
200	CY7C1386KV33-200AXC	51-85050	100-pin TQFP (14 x 20 x 1.4 mm) Pb-free	Commercial

## Ordering Code Definitions



**Package Diagrams**

**Figure 10. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050**



51-85050 \*E

## Acronyms

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
LMBU	Logical Multiple-Bit Upsets
LSB	Least Significant Bit
LSBU	Logical Single-Bit Upsets
MSB	Most Significant Bit
OE	Output Enable
SEL	Single Event Latch-Up
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mV	millivolt
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

## Document History Page

Document Title: CY7C1386KV33/CY7C1387KV33, 18-Mbit (512K x 36/1M x 18) Pipelined DCD Sync SRAM				
Document Number: 001-97893				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*B	4983482	DEVM	10/23/2015	Changed status from Preliminary to Final.
*C	5086001	DEVM	01/14/2016	Post to external web.
*D	5333184	PRIT	07/01/2016	Updated <a href="#">Neutron Soft Error Immunity</a> : Updated values in "Typ" and "Max" columns corresponding to LSBU parameter. Updated to new template.

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