



# 2-Mbit (128K words × 16 bit) Static RAM with Error-Correcting Code (ECC)

### **Features**

- High speed
  - □ t<sub>AA</sub> = 10 ns
- Temperature range
  - □ Automotive-A: -40 °C to 85 °C
     □ Automotive-E: -40 °C to 125 °C
- Embedded error-correcting code (ECC) for single-bit error correction<sup>[1]</sup>
- Low active and standby current
  - □ Active current, I<sub>CC</sub> = 40-mA typical (Automotive-E)
  - ☐ Standby current, I<sub>SB2</sub> = 6-mA typical (Automotive-E)
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- TTL compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

### **Functional Description**

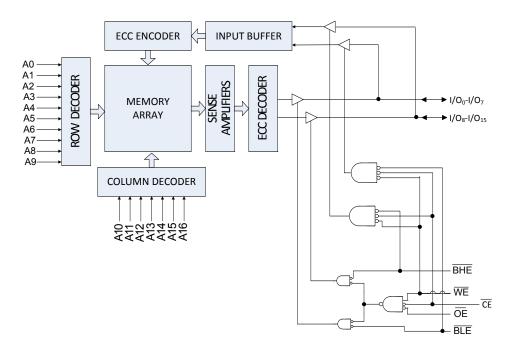
CY7C1011G is a high-performance CMOS fast static RAM automotive part with embedded ECC. This device has a single Chip Enable ( $\overline{\text{CE}}$ ) input, and is accessed by asserting it LOW.

To perform data writes, assert the Write Enable ( $\overline{\text{WE}}$ ) input LOW, and provide the data on the device data pins (I/O<sub>0</sub> through I/O<sub>15</sub>) and address pins (A<sub>0</sub> through A<sub>16</sub>) pins. The Byte High Enable ( $\overline{\text{BHE}}$ ) and Byte Low Enable ( $\overline{\text{BLE}}$ ) inputs control byte writes and write data on the corresponding I/O lines to the memory location specified. BHE controls I/O<sub>8</sub> through I/O<sub>15</sub> and BLE controls I/O<sub>0</sub> through I/O<sub>7</sub>.

To perform data reads, assert the Output Enable  $(\overline{OE})$  input and provide the required address on the address lines. You can access read data on the I/O lines (I/O $_0$  through I/O $_{15}$ ). To perform byte access, assert the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O $_0$  through I/O $_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  LOW), or when the control signals are deasserted ( $\overline{\text{OE}}$ , BLE, BHE).

# Logic Block Diagram - CY7C1011G



### Note

This device does not support automatic write-back on error detection.





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# **Pin Configurations**

Figure 1. 48-ball VFBGA (6 × 8 × 1.2 mm) pinout<sup>[2]</sup>

	1	2	3	4	5	6	_
BI	Ē	(OE)	$\bigcirc$ A <sub>0</sub>	$\bigcirc$ A <sub>1</sub>	$\bigcirc$ A <sub>2</sub>	NC	Α
(1/0	08	BHE	$\bigcirc$ A <sub>3</sub>	$\bigcirc$ A <sub>4</sub>	Œ	(I/O <sub>0</sub> )	В
(1/0	O <sub>9</sub>	(I/O <sub>10</sub> )	$\bigcirc$ A <sub>5</sub>	$\bigcirc$ A <sub>6</sub>	(I/O <sub>1</sub> )	(I/O <sub>2</sub> )	С
(VS	ss	(1/O <sub>11</sub> )	NC	$\bigcirc$ A <sub>7</sub>	(I/O <sub>3</sub> )	VCC	D
(vc	cc	(I/O <sub>12</sub> )	NC	$\left(A_{16}\right)$	(I/O <sub>4</sub> )	vss	Е
(I/C	)14)	(I/O <sub>13</sub> )	$\left(A_{14}\right)$	$\left(A_{15}\right)$	(I/O <sub>5</sub> )	(I/O <sub>6</sub> )	F
(I/C	15	NC	$\left(A_{12}\right)$	$\left(A_{13}\right)$	$\overline{\overline{\text{WE}}}$	(I/O <sub>7</sub> )	G
N	c	$\bigcirc$ A <sub>8</sub>	$\bigcirc$ A <sub>9</sub>	$\left( A_{10} \right)$	$\left( A_{11} \right)$	NC	Н
							_

Figure 2. 44-pin TSOP II pinout [2]

				1
A4 <b>■</b>	ື1		44	<b>■</b> A5
A3=	2		43	<b>■</b> A6
A2=	3		42	<b>■</b> A7
A1 <b>□</b>	4		41	<b>=</b> /OE
A0 <b>=</b>	5		40	<b>-</b> /BHE
/CE=	6		39	■ /BLE
I/O0 <b>=</b>	7		38	<b>=</b> I/O15
I/O1 =	8		37	<b>I</b> /O14
VO2 =	9	44-pin TSOP II	36	<b>■</b> I/O13
VO3 =	10	p	35	<b>I</b> /O12
VCC=	11		34	■ VSS
VSS =	12		33	■ VCC
I/O4 <b>=</b>	13		32	<b>-</b> VO11
I/O5 <b>=</b>	14		31	<b>-</b> I/O10
I/O6 <b>=</b>	15		30	<b>=</b> 1/09
I/O7 <b>=</b>	16		29	<b>-</b> 1/08
/WE <b>=</b>	17		28	■ NC
A16 🗖	18		27	<b>■</b> A8
A15 🗖	19		26	<b>=</b> A9
A14 🖿	20		25	<b>■</b> A10
A13 🗖	21		24	<b>■</b> A11
A12 🗖	22		23	■ NC

### **Product Portfolio**

				Power Dissipation				
Product	Range V <sub>CC</sub> Range (V		Speed	Operating I <sub>CC</sub> , (mA)		Standby L (mA)		
Product	Kange	V <sub>CC</sub> Range (V)	(ns)	f = f <sub>max</sub>		Standby, I <sub>SB2</sub> (mA)		
				<b>Typ</b> <sup>[3]</sup>	Max	<b>Typ</b> <sup>[3]</sup>	Max	
CY7C1011G30	Automotive -E	2.2 V-3.6 V	10	40	50	6	14	
CY/CIUTIG30	Automotive -A	2.2 V-3.0 V	10	38	45	6	8	

- NotesNC pins are not connected internally to the die.Typical values are included for reference only and are not guaranteed or tested.



# **Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ...... -65 °C to +150 °C Ambient temperature with power applied ...... -55 °C to +125 °C Supply voltage on  $V_{CC}$  relative to  $GND^{[4]}$  ......-0.5 V to Vcc +0.3 V

DC voltage applied to outputs in HI-Z State<sup>[4]</sup> ......-0.3 V to Vcc +0.3 V

DC input voltage <sup>[4]</sup>	0.3 V to V <sub>CC</sub> + 0.3 V
Current into outputs (in low state)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	>2001 V
Latch-up current	> 140 mA

# **Operating Range**

Grade	Ambient Temperature	V <sub>CC</sub>		
Automotive-E	–40 °C to +125 °C	2.2 V to 3.6 V		
Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V		

### **DC Electrical Characteristics**

Over the Operating Range

Doromotor	Description		Toot Conditions	10 ns	10 ns (Automotive-A)			10 ns (Automotive-E)		
Parameter	De	scription	Test Conditions	Min	Тур	Max	Min	Тур	Max	Unit
V <sub>OH</sub>	Output	2.2 V to 2.7 V	$V_{CC}$ = Min, $I_{OH}$ = -1.0 mA	2	_	_	2	_	-	.,
	HIGH voltage 2.7 V to 3.6 V		$V_{CC}$ = Min, $I_{OH}$ = -4.0 mA	2.2	_	_	2.2	_	_	V
$V_{OL}$	Output	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2 mA	_	_	0.4	_	-	0.4	.,
	LOW voltage	2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	_	_	0.4	_	_	0.4	V
V <sub>IH</sub>	Input	2.2 V to 2.7 V	-	2	_	$V_{CC} + 0.3^{[4]}$	2	ı	$V_{CC} + 0.3^{[4]}$	
	HIGH voltage	2.7 V to 3.6 V	_	2	_	$V_{CC} + 0.3^{[4]}$	2	_	$V_{CC} + 0.3^{[4]}$	V
V <sub>IL</sub>	Input	2.2 V to 2.7 V	-	-0.3 <sup>[4]</sup>	_	0.6	$-0.3^{[4]}$	-	0.6	.,
	LOW voltage 2.7		_	-0.3 <sup>[4]</sup>	_	0.8	-0.3 <sup>[4]</sup>	_	0.8	V
I <sub>IX</sub>	Input lea	kage current	$GND \leq V_IN \leq V_CC$	-1	_	+1	<b>-</b> 5	-	+5	μΑ
I <sub>OZ</sub>	Output le	eakage current	$\begin{aligned} &\text{GND} \leq V_{\text{OUT}} \leq V_{\text{CC}}, \\ &\text{Output disabled} \end{aligned}$	-1	_	+1	-5	-	+5	μА
I <sub>CC</sub>	Operatin current	g supply	$V_{CC}$ = 3.6 V, $I_{OUT}$ = 0 mA, CMOS levels $f = f_{MAX} = \frac{1}{t_{RC}}$	_	38	45	_	40	50	mA
I <sub>SB1</sub>	Automatic CE power down current – TTL inputs		$V_{CC} = 3.6 \text{ V}, \overline{CE} \ge V_{IH},$ $V_{IN} \ge V_{IH} \text{ or } V_{IN} \le V_{IL},$ $f = f_{MAX}$	-	_	15	-	_	24	mA
I <sub>SB2</sub>		Automatic CE power down current – CMOS V <sub>CC</sub> = 3.6 V,		-	6	8	-	6	14	mA

### Note

Document Number: 001-95423 Rev. \*B

<sup>4.</sup>  $V_{IL(min)}$  = -2.0 V and  $V_{IH(max)}$  =  $V_{CC}$  + 2 V for pulse durations of less than 2 ns.



# Capacitance

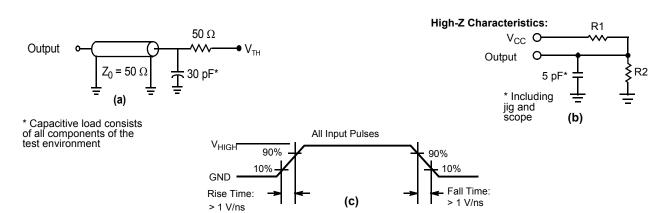
Parameter [5]	Description	Test Conditions	All Packages	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25 ^{\circ}\text{C}$ , $f = 1 \text{MHz}$ , $V_{CC} = V_{CC(typ)}$	10	pF
C <sub>OUT</sub>	I/O capacitance		10	pF

### **Thermal Resistance**

Param	eter [5]	Description	Test Conditions	48-ball VFBGA	44-pin TSOPII	Unit
$\Theta_{JA}$			Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	30.68	66.82	°C/W
$\Theta_{\sf JC}$		Thermal resistance (junction to case)		14.83	15.97	°C/W

### **AC Test Loads and Waveforms**

Figure 3. AC Test Loads and Waveforms [6]



Parameters	3.0 V	Unit
R1	317	Ω
R2	351	Ω
V <sub>TH</sub>	1.5	V
V <sub>HIGH</sub>	3	V

### Notes

- 5. Tested initially and after any design or process change that may affect these parameters.
  6. Full-device AC operation assumes a 100-µs ramp time from 0 to V<sub>CC(min)</sub> and a 100-µs wait time after V<sub>CC</sub> stabilization.



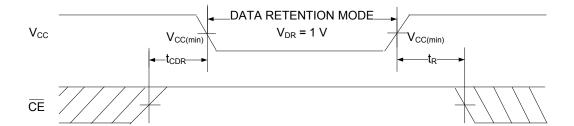
# **Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions	Autom	otive-A	Autom	11:0:4	
			Min	Max	Min	Max	Unit
$V_{DR}$	V <sub>CC</sub> for data retention	_	1	-	1	_	V
I <sub>CCDR</sub>	Data retention current	$V_{CC} = 1.2 \text{ V}, \overline{CE} \ge V_{CC} - 0.2 \text{ V},$ $V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$	_	8	_	14	mA
t <sub>CDR</sub> <sup>[7]</sup>	Chip deselect to data retention time	_	0	-	0	_	ns
t <sub>R</sub> <sup>[7, 8]</sup>	Operation recovery time	V <sub>CC</sub> ≥ 2.2 V	10	_	10	_	ns

# **Data Retention Waveform**

Figure 4. Data Retention Waveform<sup>[8]</sup>



Notes
7. These parameters are guaranteed by design.
8. Full-device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \ge 100~\mu s$  or stable at  $V_{CC(min.)} \ge 100~\mu s$ .



# **AC Switching Characteristics**

Over the Operating Range

Parameter [9]	Description	10 ns (Auto	10 ns (Automotive-A/ Automotive-E)		
	·	Min	Min Max		
Read Cycle		· · · · · · · · · · · · · · · · · · ·		•	
t <sub>RC</sub>	Read cycle time	10	_	ns	
t <sub>AA</sub>	Address to data	-	10	ns	
t <sub>OHA</sub>	Data	3	-	ns	
t <sub>ACE</sub>	CE LOW to data [9]	-	10	ns	
t <sub>DOE</sub>	OE LOW to data	-	4.5	ns	
t <sub>LZOE</sub>	OE LOW to low impedance [10, 11]	0	-	ns	
t <sub>HZOE</sub>	OE HIGH to HI-Z [10, 11]	-	5	ns	
t <sub>LZCE</sub>	CE LOW to low impedance [9, 10, 11]	3	_	ns	
t <sub>HZCE</sub>	CE HIGH to HI-Z [9, 10, 11]	-	5	ns	
t <sub>PU</sub>	CE LOW to power up [9, 11]	0	_	ns	
t <sub>PD</sub>	CE HIGH to power down [9, 11]	_	10	ns	
t <sub>DBE</sub>	Byte enable to data valid	_	4.5	ns	
t <sub>LZBE</sub>	Byte enable to low impedance <sup>[11]</sup>	0	_	ns	
t <sub>HZBE</sub>	Byte disable to HI-Z <sup>[11]</sup>	-	6	ns	
Write Cycle [12	, 13]	<u> </u>			
t <sub>WC</sub>	Write cycle time	10	_	ns	
t <sub>SCE</sub>	CE LOW to write end [9]	7	_	ns	
t <sub>AW</sub>	Address setup to write end	7	_	ns	
t <sub>HA</sub>	Address hold from write end	0	_	ns	
t <sub>SA</sub>	Address setup to write start	0	_	ns	
t <sub>PWE</sub>	WE pulse width	7	_	ns	
t <sub>SD</sub>	Data setup to write end	5	_	ns	
t <sub>HD</sub>	Data hold from write end	0	_	ns	
t <sub>LZWE</sub>	WE HIGH to low impedance [10, 11]	3	_	ns	
t <sub>HZWE</sub>	WE LOW to HI-Z [10, 11]	_	5	ns	
t <sub>BW</sub>	Byte Enable to write end	7	_	ns	

<sup>9.</sup> Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V<sub>CC</sub> ≥ 3 V) and V<sub>CC</sub>/2 (for V<sub>CC</sub> < 3 V), and input pulse levels of 0 to 3 V (for V<sub>CC</sub> ≥ 3 V) and 0 to V<sub>CC</sub> (for V<sub>CC</sub> < 3 V). Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 5, unless specified otherwise.</li>
10. t<sub>HZOE</sub>, t<sub>HZOE</sub>, t<sub>HZOE</sub>, t<sub>HZOE</sub>, t<sub>LZOE</sub>, t<sub>LZOE</sub>, t<sub>LZOE</sub>, and t<sub>LZBE</sub> are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 5. Transition is measured ±200 mV from steady state voltage.
11. These parameters are guaranteed by design and are not tested.
12. The internal write time of the memory is defined by the overlap of WE = V<sub>IL</sub>, CE = V<sub>IL</sub> and BHE or BLE = V<sub>IL</sub>. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

<sup>13.</sup> The minimum write cycle pulse width for Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) should be equal to sum of  $t_{\text{ND}}$  and  $t_{\text{HZWE}}$ .



# **Switching Waveforms**

Figure 5. Read Cycle No. 1 of CY7C1011G (Address Transition Controlled) [14, 15]

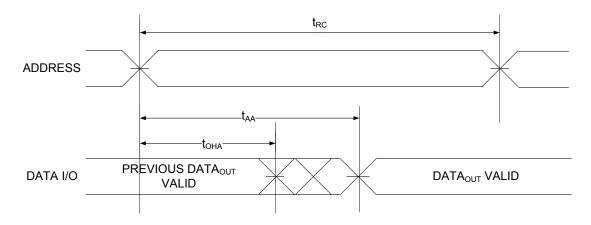
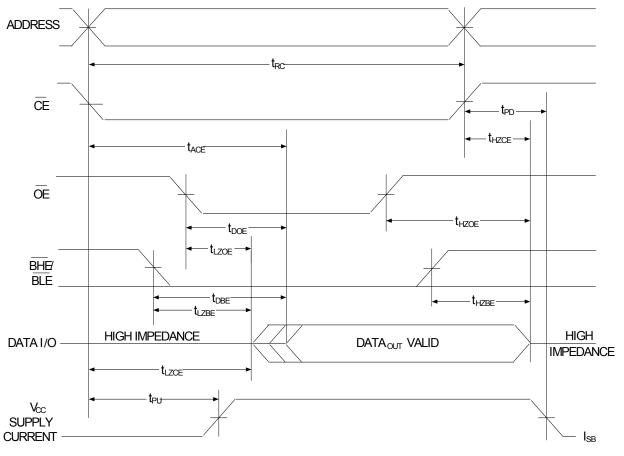


Figure 6. Read Cycle No. 2 (OE Controlled) [15]



<sup>14.</sup> The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ . 15.  $\overline{WE}$  is HIGH for read cycle.



### Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (CE Controlled) [16, 17, 18]

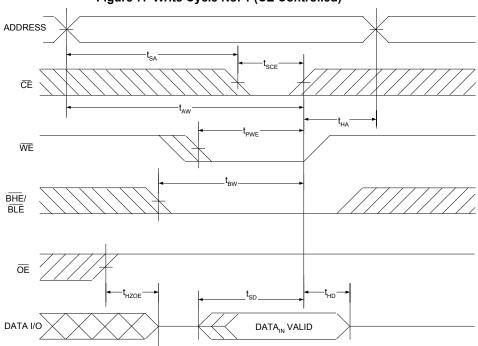
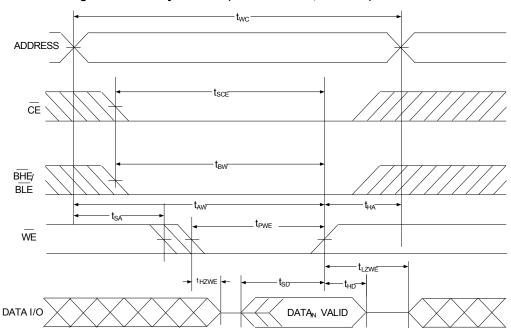


Figure 8. Write Cycle No. 2 (WE Controlled, OE LOW) [16, 17, 18, 19]



### Notes

- 16. Address valid prior to or coincident with  $\overline{\text{CE}}$  LOW transition.
- 17. The internal write time of the memory is defined by the overlap of WE = V<sub>IL</sub>, CE = V<sub>IL</sub> and BHE or BLE = V<sub>IL</sub>. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates
- 18. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .

  19. The minimum write cycle pulse width should be equal to sum of  $t_{SD}$  and  $t_{HZWE}$ .



### Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 (BLE or BHE Controlled) [20, 21]

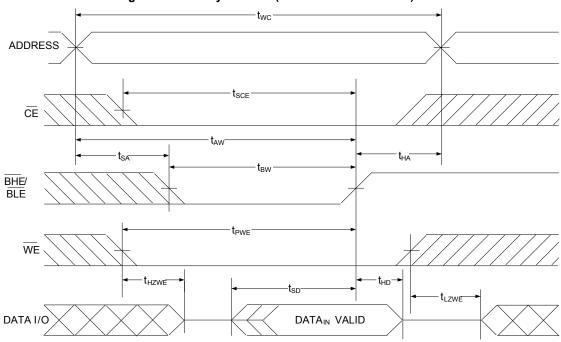
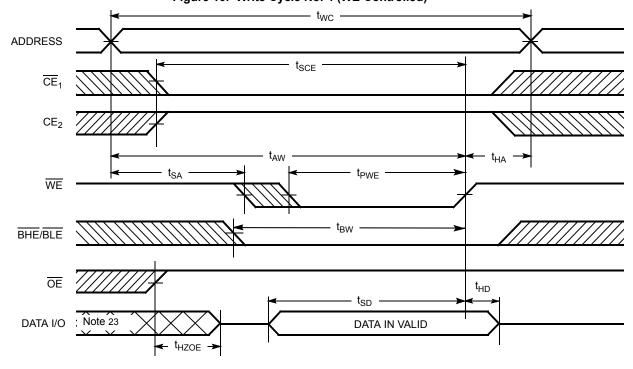


Figure 10. Write Cycle No. 4 (WE Controlled) [20, 21, 22]



### Notes

- 20. The internal write time of the memory is defined by the overlap of WE = V<sub>IL</sub>, CE = V<sub>IL</sub> and BHE or BLE = V<sub>IL</sub>. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 21. Data I/O is in HI-Z state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ . 22. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
- 23. During this period the I/Os are in output state. Do not apply input signals.



# **Truth Table**

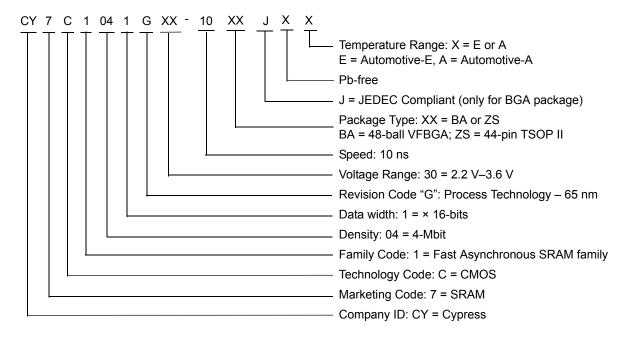
CE	ŌE	WE	BLE	BHE	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
Н	Х	Х	Х	Х	HI-Z	HI-Z	Power-down	Standby (I <sub>SB</sub> )
L	L	Н	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	L	Н	L	Н	Data out	HI-Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	Н	Н	L	HI-Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	Х	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	Х	L	L	Н	Data in	HI-Z	Write lower bits only	Active (I <sub>CC</sub> )
L	Х	L	Н	L	HI-Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	Н	Н	Х	Х	HI-Z	HI-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )



# **Ordering Information**

Speed (ns)	Ordering Code	Voltage Range	Package Diagram	Package Type (All Pb-free)	Operating Range
10	CY7C1011G30-10BAJXE	2.2 V-3.6 V	001-85259	48-ball VFBGA	Automotive-E
	CY7C1011G30-10ZSXE	2.2 V-3.6 V	51-85087	44-pin TSOP II	Automotive-E
	CY7C1011G30-10ZSXA	2.2 V-3.6 V	51-85087	44-pin TSOP II	Automotive-A

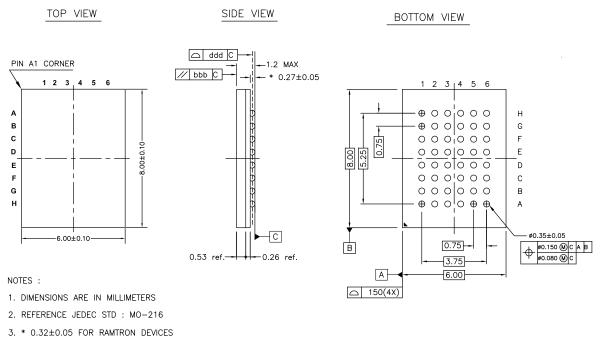
### **Ordering Code Definitions**





# **Package Diagrams**

Figure 11. 48-ball VFBGA (6 × 8 × 1.2 mm) BA48M/BK48M (0.35 mm Ball Diameter) Package Outline, 001-85259

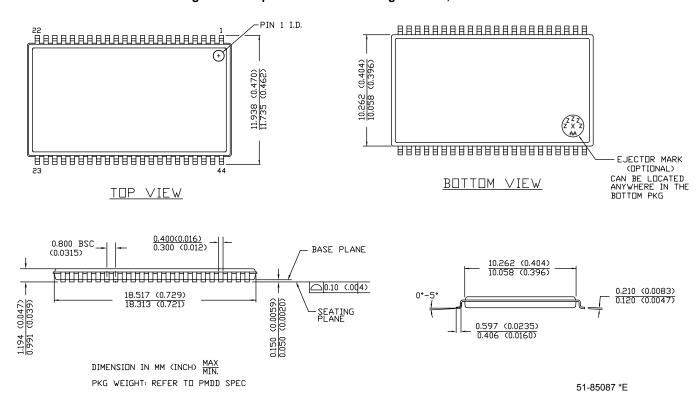


001-85259 \*A



### Package Diagrams (continued)

Figure 12. 44-pin TSOP Z44-II Package Outline, 51-85087





# Acronyms

Acronym	Description			
BHE	Byte High Enable			
BLE	Byte Low Enable			
CE	Chip Enable			
CMOS	Complementary Metal Oxide Semiconductor			
I/O	Input/Output			
ŌĒ	Output Enable			
SRAM	Static Random Access Memory			
TSOP	Thin Small Outline Package			
TTL	Transistor-Transistor Logic			
VFBGA	Very Fine-Pitch Ball Grid Array			
WE	Write Enable			

### **Document Conventions**

### **Units of Measure**

Symbol	Unit of Measure				
°C	degrees Celsius				
MHz	megahertz				
μΑ	microampere				
μS	microsecond				
mA	milliampere				
mm	millimeter				
ns	nanosecond				
Ω	ohm				
%	percent				
pF	picofarad				
V	volt				
W	watt				



# **Document History Page**

Document Title: CY7C1011G Automotive, 2-Mbit (128K words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-95423					
Rev. ECN No. Orig. of Change Date			Description of Change		
*A	4998910	NILE	11/02/2015	Changed status from Preliminary to Final.	
*B	5024020	NILE	11/23/2015	Updated Ordering Information: Updated part numbers.	



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# **Technical Support**

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