



ALPHA & OMEGA
SEMICONDUCTOR



AOD450 N-Channel Enhancement Mode Field Effect Transistor

General Description

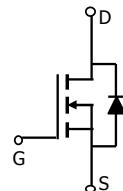
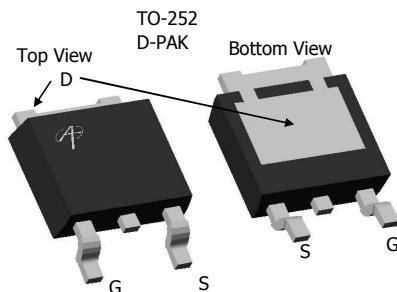
The AOD450 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in inverter, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free*

Features

V_{DS} (V) = 200V
 I_D = 3.8A (V_{GS} = 10V)
 $R_{DS(ON)} < 0.7\Omega$ (V_{GS} = 10V)

100% UIS Tested!
100% R_g Tested!



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	$T_C=25^\circ C$	3.8	A
Current		2.7	
Pulsed Drain Current ^C	I_{DM}	10	
Avalanche Current ^C	I_{AR}	3	A
Repetitive avalanche energy $L=1.35mH$ ^C	E_{AR}	6	mJ
Power Dissipation ^B	$T_C=25^\circ C$	25	W
		12.5	
Power Dissipation ^A	$T_A=25^\circ C$	2.1	W
		1.3	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$t \leq 10s$	$R_{\theta JA}$	17.1	°C/W
Maximum Junction-to-Ambient ^A	Steady-State		50	°C/W
Maximum Junction-to-Case ^B	Steady-State	$R_{\theta JC}$	4	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=10\text{mA}, V_{GS}=0\text{V}$	200			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=160\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		1	5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm30\text{V}$			100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	3	5	6	V
$I_{D(\text{ON})}$	On state drain current	$V_{GS}=10\text{V}, V_{DS}=15\text{V}$	10			A
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=3.8\text{A}$ $T_J=125^\circ\text{C}$	0.55 1.1	0.70 1.32		Ω
g_{FS}	Forward Transconductance	$V_{DS}=15\text{V}, I_D=3.8\text{A}$		8.7		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.8	1	V
I_S	Maximum Body-Diode Continuous Current ^G				6	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1\text{MHz}$		215		pF
C_{oss}	Output Capacitance			32		pF
C_{rss}	Reverse Transfer Capacitance			7.2		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		5.5		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=25\text{V}, I_D=3.8\text{A}$		3.82		nC
$Q_g(4.5\text{V})$	Total Gate Charge			0.92		nC
Q_{gs}	Gate Source Charge			1.42		nC
Q_{gd}	Gate Drain Charge			1.47		nC
$t_{D(\text{on})}$	Turn-On DelayTime	$V_{GS}=10\text{V}, V_{DS}=25\text{V}, R_L=6.5\Omega, R_{\text{GEN}}=3\Omega$		6.3		ns
t_r	Turn-On Rise Time			3.3		ns
$t_{D(\text{off})}$	Turn-Off DelayTime			10.5		ns
t_f	Turn-Off Fall Time			2.8		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=3.8\text{A}, dI/dt=100\text{A}/\mu\text{s}$		59		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=3.8\text{A}, dI/dt=100\text{A}/\mu\text{s}$		142		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature to 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(\text{MAX})}=175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})}=175^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(\text{MAX})}=175^\circ\text{C}$.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev1: Sep 2008

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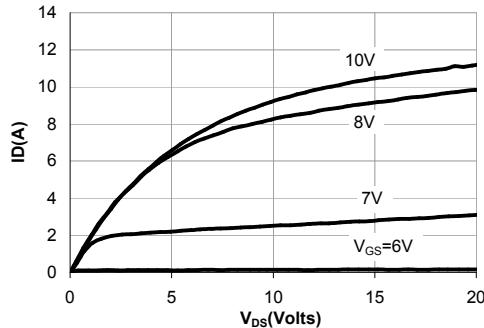
TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1: On-Region Characteristics

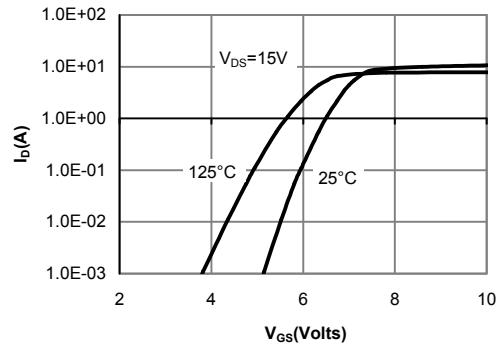


Figure 2: Transfer Characteristics

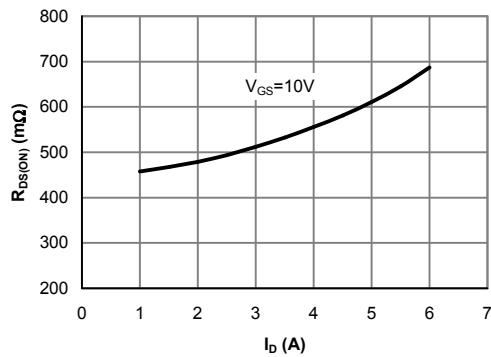


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

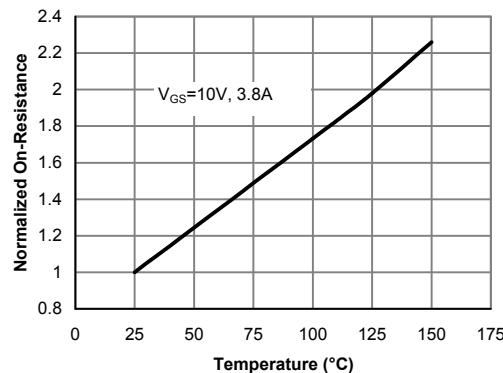


Figure 4: On-Resistance vs. Junction Temperature

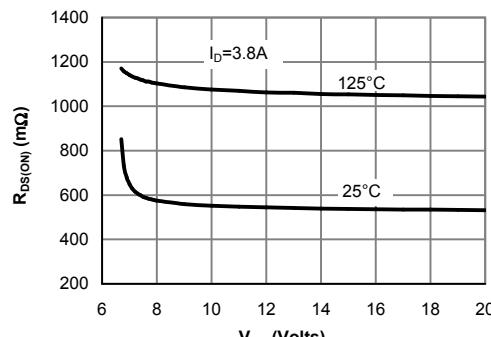


Figure 5: On-Resistance vs. Gate-Source Voltage

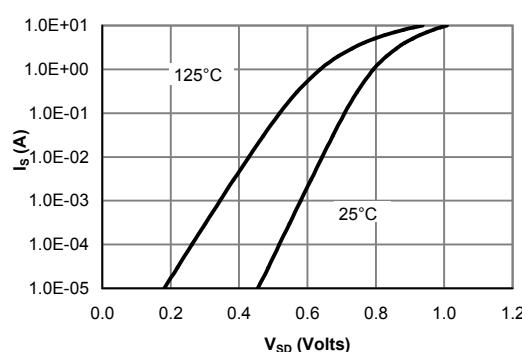


Figure 6: Body-Diode Characteristics

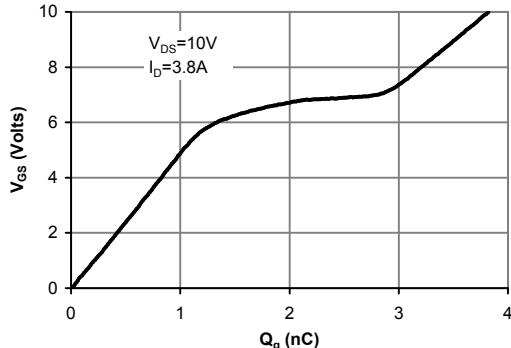
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 7: Gate-Charge Characteristics

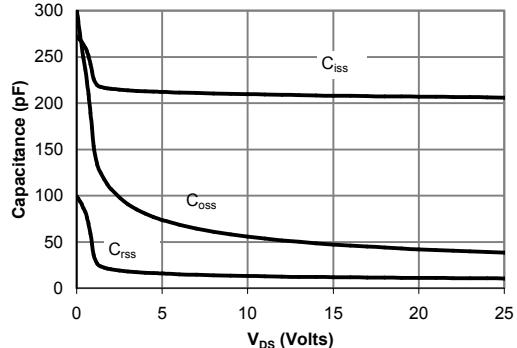


Figure 8: Capacitance Characteristics

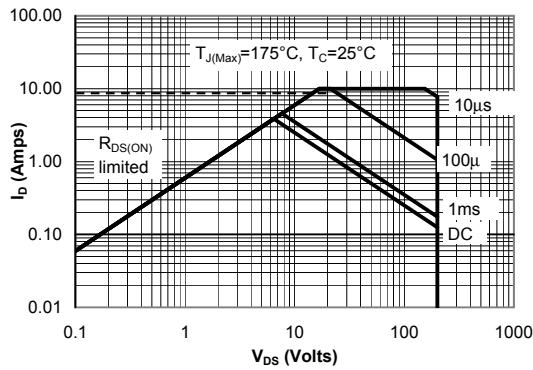


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

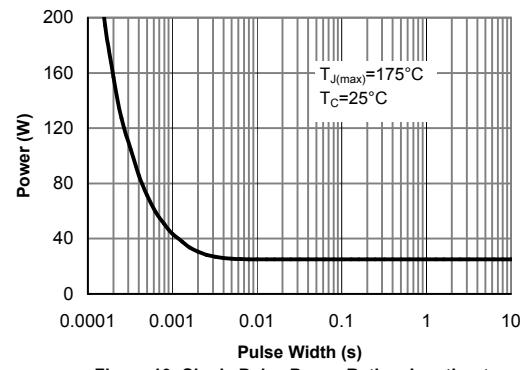


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

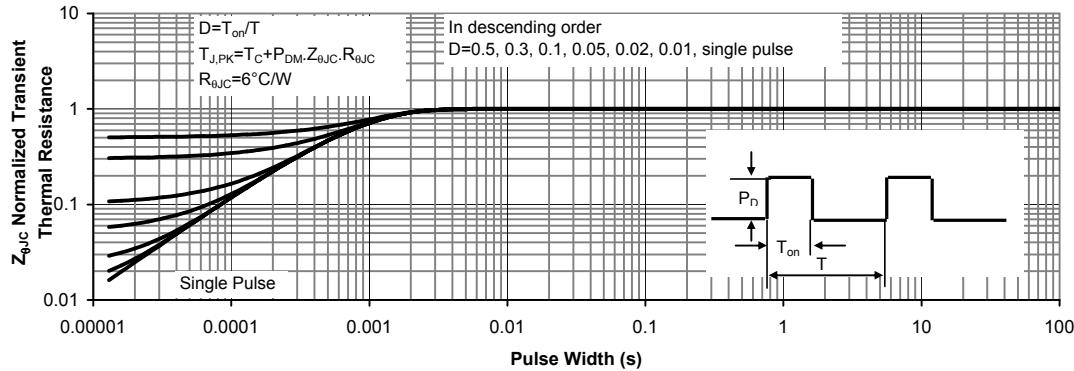


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

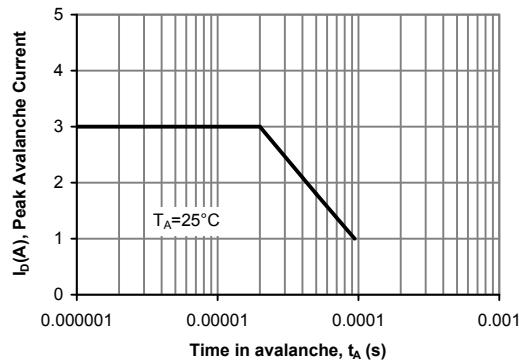
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 12: Single Pulse Avalanche capability

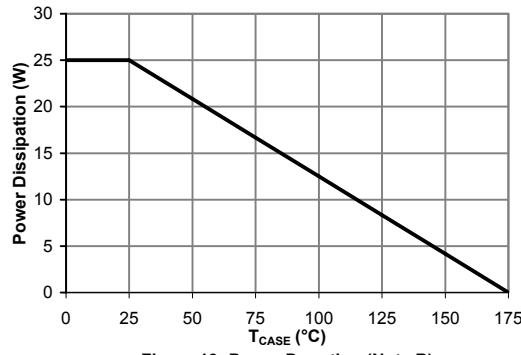


Figure 13: Power De-rating (Note B)

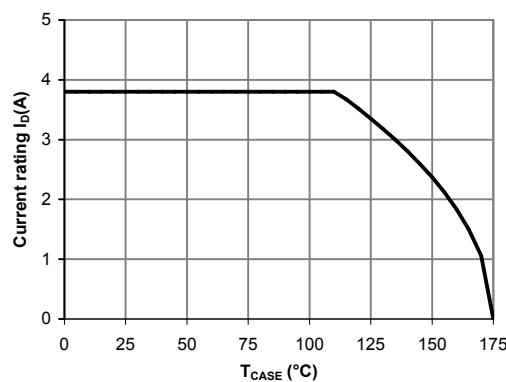


Figure 14: Current De-rating (Note B)

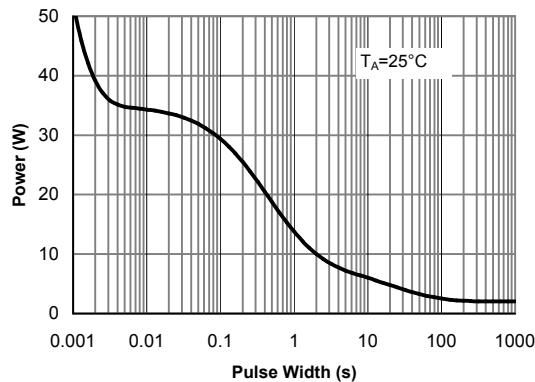


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

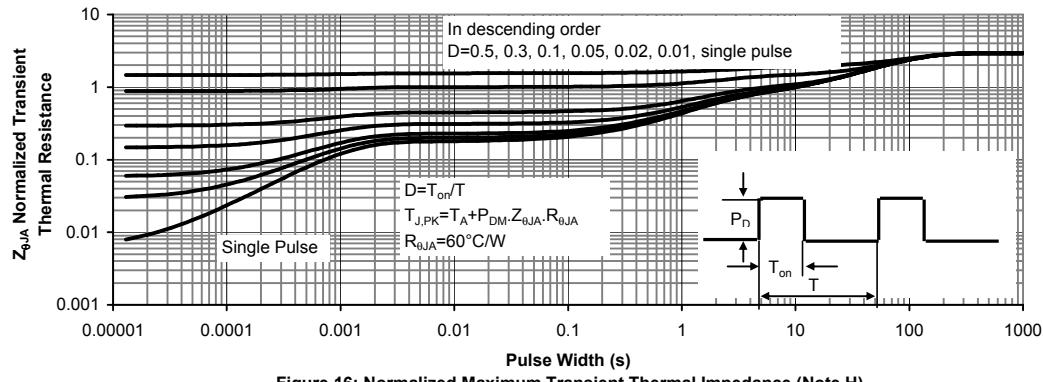
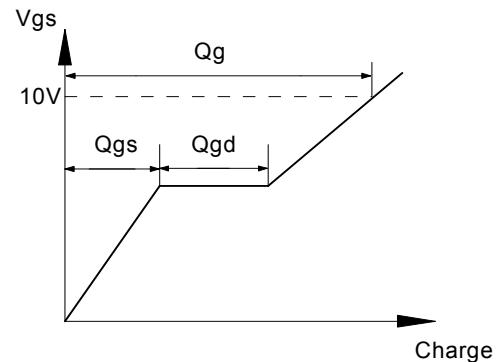
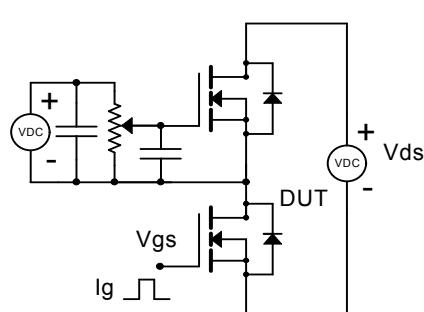
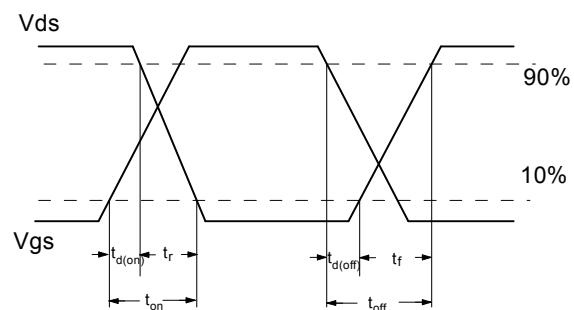
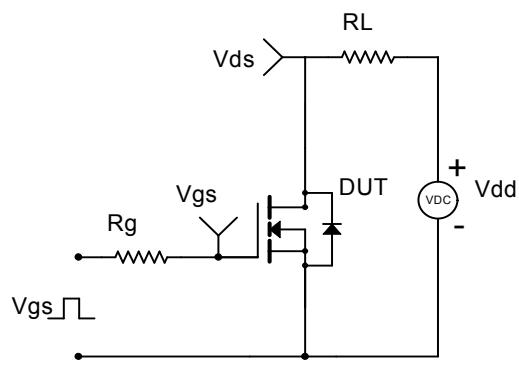


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

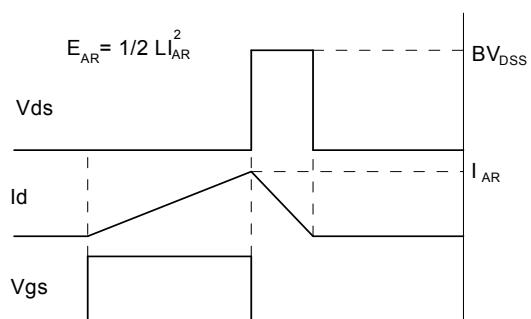
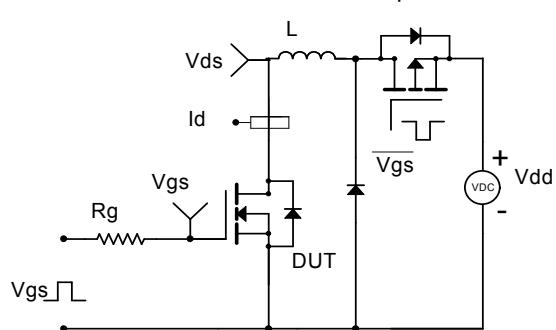
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

