



MICROCHIP PIC18F2480/2580/4480/4580

PIC18F2480/2580/4480/4580 Data Sheet Errata

Clarifications/Corrections to the Data Sheet

In the PIC18F2480/2580/4480/4580 Device Data Sheet (DS39637C), the following clarifications and corrections should be noted. Any silicon issues related to this device will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Enhanced Capture/Compare PWM (ECCP1)

The following note has been added to the end of **Section 16.4.6 “Programmable Dead-Band Delay”**.

Note: If the dead-band delay value is increased after the dead-band time has elapsed, that new value takes effect immediately. This happens even if the PWM pulse is high and can appear to be a glitch. Dead-band values must be changed during the dead-band time or before ECCP is active.

2. Module: Master Synchronous Serial Port (MSSP) – Serial Peripheral Interface (SPI)

The following note has been added to the end of **Section 17.3.3 “Enabling SPI I/O”**.

Note: When the module is enabled and in Master mode (CKE, SSPSTAT<6> = 1), a small glitch of approximately half a T_{CY} may be seen on the SCK pin. To resolve this, keep the SCK pin as an input while setting SPEN. Then, configure the SCK pin as an output (TRISC<3> = 0).

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3. Module: Electrical Characteristics (DC Supply Voltage)

Note 2 is added to Section 27.1 “DC Characteristics: Supply Voltage” pertaining to parameter D005.

27.1 DC Characteristics: Supply Voltage PIC18F2480/2580/4480/4580 (Industrial, Extended) PIC18LF2480/2580/4480/4580 (Industrial)

PIC18LF2480/2580/4480/4580 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F2480/2580/4480/4580 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D001	VDD	Supply Voltage					
		PIC18LF2X80/4X80	2.0	—	5.5	V	
		PIC18F2X80/4X80	4.2	—	5.5	V	
D002	VDR	RAM Data Retention Voltage⁽¹⁾	1.5	—	—	V	
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	—	0.7	V	See section on Power-on Reset for details
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Reset Voltage					
		PIC18LF2X80/4X80					
		BORV1:BORV0 = 11	2.00	2.05	2.16	V	
		BORV1:BORV0 = 10	2.65	2.79	2.93	V	
D005		All Devices					
		BORV1:BORV0 = 01 ⁽²⁾	4.11	4.33	4.55	V	
		BORV1:BORV0 = 00	4.36	4.59	4.82	V	

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

Note 2: With BOR enabled, full-speed operation (FOSC = 40 MHz) is supported until a BOR occurs. This is valid, although VDD may be below the minimum voltage for this frequency.

REVISION HISTORY

Rev A Document (03/2006)

Original version of this document. Includes Data Sheet Clarification issue 1 (Flash Program Memory – Erase Block), 2 (Flash Program Memory – Pointer Boundaries), 3 (Figure 6-2: Table Write Operation), 4 (Section 6.2.4 Table Pointer Boundaries) 5 (Section 6.5 Writing to Flash Program Memory) 6 (Section 6.5.1 Flash Program Memory Write Sequence) and 7 (Example 6-3: Writing to Flash Program Memory).

Rev B Document (11/2007)

Removed Data Sheet Clarification issues 1-7 (Flash Program Memory) and added new issues 1 (ECCP1) and 2 (MSSP – SPI).

Rev C Document (2/2009)

Added Data Sheet Clarification issue 3 (Electrical Characteristics – DC Supply Voltage).

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NOTES:

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