

MC9328MX21S Applications Processor

Freescale's i.MX family of microprocessors has demonstrated leadership in the portable handheld market. Building on the success of the MX (Media Extensions) series, the i.MX21S (MC9328MX21S) provides a leap in performance with an ARM926EJ-S™ microprocessor core that provides accelerated Java support in addition to highly integrated system functions. The i.MX21S device addresses the needs of multiple markets with intelligent integrated peripherals, advanced ARM® processor core, and power management capabilities.

The i.MX21S features the advanced and power-efficient ARM926EJ-S core operating at speeds up to 266 MHz and is part of a growing family of *Smart Speed* products that offer high performance processing optimized for lowest power consumption. On-chip modules such as an LCD controller, USB On-The-Go, 1-Wire® interface, and synchronous serial interfaces offer designers a rich suite of peripherals that can enhance many products.

For cost sensitive applications, the NAND Flash controller allows the use of low cost Nand Flash devices to be used as primary or secondary non-volatile storage. The on-chip ECC and parity checking circuitry of the

Contents

1 i.MX21S Block Diagram	2
2 i.MX21S Features	3
2.1 ARM926EJ-S Core Complex	3
2.2 System Control and Timers	4
2.3 Memory Interface	5
2.4 Inter-Chip Connectivity	7
2.5 Display and Video Modules	8
2.6 Two Multimedia Card and Secure Digital Host Controller Modules	9
2.7 Digital Audio Mux	9
2.8 Connectivity and Expansion	9
2.9 Debug Capability	11
2.10 Power Management	14
2.11 Electronic and Package Information	14
3 Document Revision History	14



Nand Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The i.MX21S processor is packaged in a 289-pin molded array process ball grid array (MAPBGA).

A summary of the main features of the i.MX21S processor includes:

- High level of on-chip integration
- Very low-power system design without compromised performance
- Optimized for Bluetooth applications with high-speed interfaces to external Bluetooth solutions

1 i.MX21S Block Diagram

Figure 1 is a simplified functional block diagram of the i.MX21S processor.

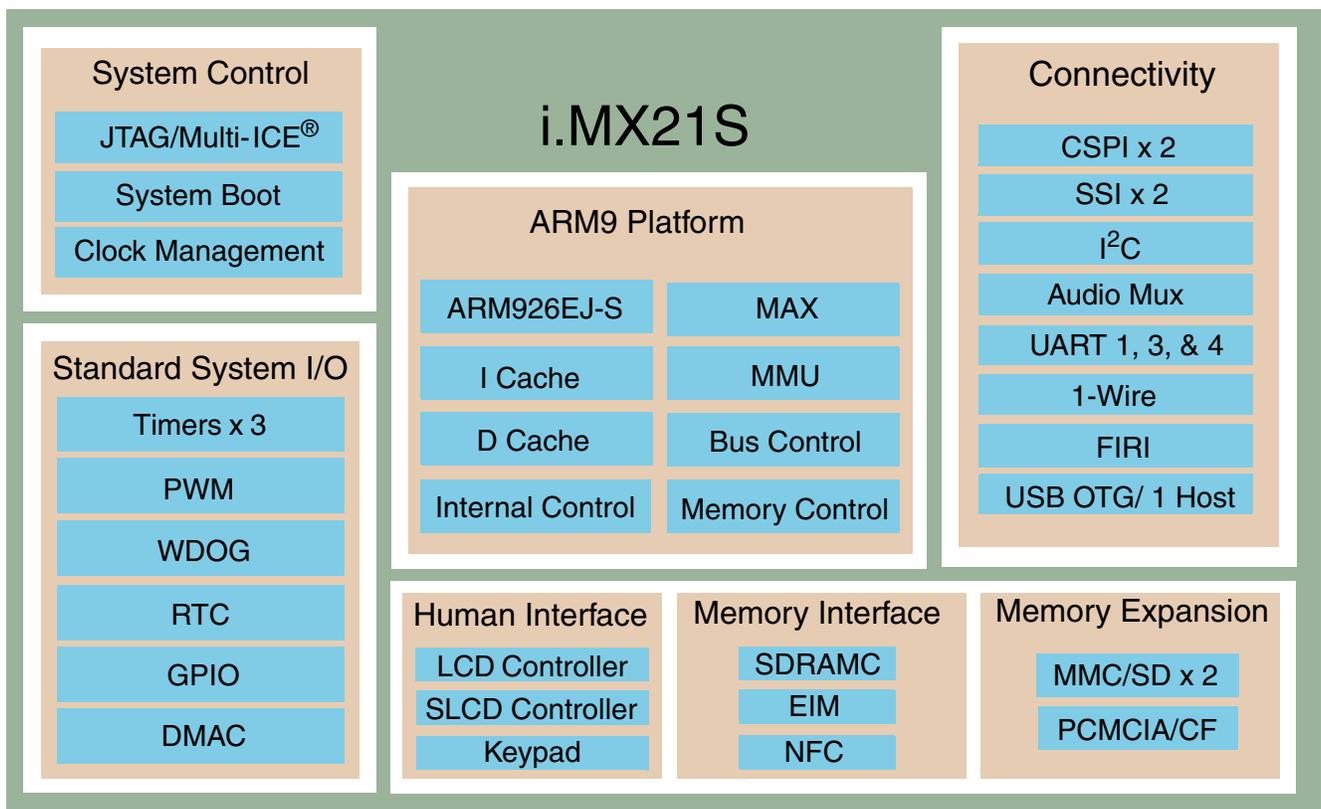


Figure 1. i.MX21S Functional Block Diagram

2 i.MX21S Features

The MC9328MX21S boasts a robust array of features that can support a wide variety of applications. This section provides a brief description of these features.

2.1 ARM926EJ-S Core Complex

The ARM926EJ-S Core Complex (also known as the ARM926 Platform) consists of the ARM926EJ-S processor, a 6 × 4 Multi-Layer AHB crossbar switch, and a primary AHB complex.

- ARM926EJ-S microprocessor core
 - 16K instruction cache and 16K data cache
 - High-performance ARM® 32-bit RISC engine
 - Thumb® 16-bit compressed instruction set for a leading level of code density
 - Efficient execution of Java byte codes
 - EmbeddedICE™ JTAG software debug
 - 100 percent user code binary compatibility with ARM7TDMI™
 - Advanced Microcontroller Bus Architecture (AMBA™) system-on-chip multi-master bus interface
 - Support for mixed loads of real-time and user applications via cache locking facilities
 - Virtual Memory Management Unit (VMMU)
- ARM Interrupt Controller (AITC)
 - The AITC is connected to the primary AHB as a slave device and provides support for up to 64 interrupt sources. It generates normal and fast interrupts to the processor core. The AITC supports a hardware assisted vectoring mode for automatic vectoring to reduce interrupt latency.
- Digital Phase-Locked Loops (DPLLs) and Power Control Module
 - Digital phase-locked loops (DPLLs) and clock controller for all internal clock generation
 - MCUPLL generates system and CPU clocks from a 26MHz crystal
 - USBPLL generates 48 MHz clock for the USB OTG from either a 26 MHz crystal or 32kHz
 - Support for three power modes for different power consumption needs: run, doze, and stop.
- AHB to IP bus interfaces (AIPIs)
 - Provide a communication interface between the high-speed AHB to a lower-speed IP bus for slave peripherals
- The Multi-Layer 6 × 4 AHB Crossbar Switch
 - The crossbar switch allows for concurrent transactions to proceed from any input port (bus master) to any output port (bus slave). That is, it is possible for all four output ports to be active at the same time as a result of four independent input or output requests.
- CPU and System speed
 - ARM926EJ-S core: up to 266 MHz
 - System Clock: up to 133 MHz

- External memory interface: same clock source as system, up to 133 MHz at 1.8V supply
- System clock is derived from the CPU clock through an integer divider

2.2 System Control and Timers

The i.MX21S processor contains various timers and system control features to optimize the control of both the internal modules and external devices.

2.2.1 Watchdog Timer

The Watchdog Timer module (WDOG Timer) provides the following:

- Programmable time out of 0.5 s to 64 s
- Resolution of 0.5 s

2.2.2 Real-Time Clock/Sampling Timer

The Real-Time Clock (RTC) module maintains the system clock, provides stopwatch, alarm, and interrupt functions, and supports the following features:

- 32.768 kHz and 32 kHz input operation
- Full clock features: seconds, minutes, hours, days
- Capable of counting up to 512 days
- Minute countdown timer with interrupt
- Programmable daily alarm with interrupt
- Sampling timer with interrupt
- Once-per-second, once-per-minute, once-per-hour, and once-per-day interrupts
- Interrupt generation for digitizer sampling or keyboard debouncing

2.2.3 Three General-Purpose 32-Bit Counters/Timers

The General-Purpose Timer (GPT) module contains three identical general-purpose 32-bit timers with programmable prescalers and compare and capture registers with the following features:

- Automatic interrupt generation
- Programmable timer input/output pins
- Input capture capability with programmable trigger edge
- Output compare with programmable mode

2.2.4 Pulse-Width Modulator Module

The following features characterize the Pulse-Width Modulator (PWM) module:

- 4 × 16 FIFO to minimize interrupt overhead
- 16-bit resolution
- Sound and melody generation

2.2.5 General-Purpose I/O Ports

The GPIO module provides six general purpose I/O ports. Each single GPIO port is a 32-bit port that may be multiplexed with one or more dedicated functions. The GPIO features are:

- Supports level or edge trigger interrupt and is system wake-up capable
- Most I/O signals are multiplexed with dedicated functions for pin efficiency

2.2.6 Endianness

The i.MX21S processor system supports little endian only.

2.3 Memory Interface

The memory interfaces of the i.MX21S processor consist of the SDRAM controller, the Direct Memory Access controller, the NAND Flash controller and the External Interface module. The individual features of these controllers are provided in this section.

2.3.1 SDRAM Controller

The SDRAM controller (SDRAMC) consists of 7 major blocks, including the SDRAM command controller, page and bank address comparators, row/column address multiplexer, data aligner/multiplexer, configuration registers, refresh request counter, and the powerdown timer.

The features offered by the SDRAMC are as follows:

- Support for four banks of single data rate 64 Mbit, 128 Mbit, and 256 Mbit SDRAM
 - Two independent chip-selects with up to 64 Mbyte per chip-select
 - Up to four banks active simultaneously for each chip-select
 - JEDEC standard pinout and operation
 - Boot capability from CSD1
- PC133-compliant interface
 - 133 MHz system clock achievable with “-8” option PC133-compliant memories
 - Single and fixed-length (4-word) burst access
 - Access time of 8-1-1-1 at 133 MHz
- Software configurable for differing system requirements
 - 16-bit or 32-bit bus width
 - Configurable row cycle delay (tRC), row precharge delay (tRP), row-to-column delay (tRCD), and column-to-data delay (CAS latency)
- Built-in auto-refresh timer and state machine
- Hardware-supported self-refresh entry and exit: capability to maintain valid data during system reset and low-power modes
- Auto-powerdown (clock suspend) timer

2.3.2 Direct Memory Access Controller

The Direct Memory Access Controller (DMAC) provides 16 channels to support linear memory, 2D memory, FIFO and end-of-burst enable FIFO transfers to support a wide variety of DMA operations. Features include:

- Supports 16 channels linear memory, 2D memory and FIFO for both source and destination
- Supports 8-bit, 16-bit, or 32-bit FIFO port size and memory port size data transfer
- DMA burst length is configurable up to maximum of 16 words, 32 half-words, or 64 bytes for each channel
- Bus utilization control for a channel that is not triggered by DMA request
- Interrupts provided to interrupt handler on bulk data transfer complete or transfer error
- DMA burst time-out error to terminate DMA cycle when the burst cannot be completed in a programmed timing period
- Dedicated external DMA request and grant signal
- Support increment, decrement and no increment for source and destination addressing
- Supports DMA chaining

2.3.3 NAND Flash Controller

The NAND Flash controller (NFC) interfaces standard NAND Flash parts to the i.MX21S processor and hides the complexities of accessing NAND Flash. The NFC features include:

- Contains hardware bootloader for automatic boot up from NAND Flash devices
- Supports all 8-bit/16-bit NAND Flash devices regardless of density and organization
- Supports 512 byte and 2 Kbyte page sizes
- Internal 2 Kbyte of buffer RAM used as boot RAM during cold startup and as read/write page buffers to relieve CPU intervention
- Automatic ECC detection and selectable correction
- Data protection for ram buffer and NAND Flash pages

2.3.4 External Interface Module

The External Interface module (EIM) handles the interface to devices external to the i.MX21S processor, including generation of chip selects for external peripherals and memory, and provides the following features:

- Six Chip Selects (CS0-5) for external devices, each with 16 Mbyte of address space
- CS0 supports boot from ROM, NAND, or NOR Flash of up to 32 Mbyte of address space
- Programmable protection, port size, and wait states for each chip-select
- Internal/external boot ROM selection
- Selectable bus watchdog counter
- Burst support for external AMD™ or Intel® flash with 32-bit data path
- External Data Transfer Acknowledge (DTACK) support for slower devices connected on CS5

2.4 Inter-Chip Connectivity

This section describes how the modules within the i.MX21S processor interface with each other and provides a high-level overview on how the architecture of the busses are configured and multiplexed.

2.4.1 Inter-IC (I²C) Bus Module

I²C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I²C allows additional devices to be connected to the bus for expansion and system development. The I²C features include:

- Multiple-master operation
- Software-programmable for 1 of 64 different serial clock frequencies
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation and detection
- Repeated START signal generation
- Acknowledge bit generation and detection
- Bus-busy detection

2.4.2 Two Configurable Serial Peripheral Interfaces for High Speed Data Transfer

The i.MX21S processor has two Configurable Serial Peripheral Interface (CSPI) modules that allow rapid data communication with fewer software interrupts than conventional serial communications.

The primary features of the CSPIs include:

- Master/slave configurable (CSPI1 and CSPI2 only)
- Three available chip-selects (CSPI1 and CSPI2) for master mode operation (SS0–SS2)
- Up to 32-bit programmable data transfer
- 8 × 32 FIFO for both transmit and receive data

2.4.3 Two Synchronous Serial Interfaces with Inter-IC Sound (I²S) and AC97 Host Controller Module (SSI/I²S/AC97)

Features include the following:

- Supports generic SSI interface for timeslot based communication with synchronous voice codecs
- Timeslot mode supports up to 4 channels for communication among devices Bluetooth voice port, voice codecs and baseband audio ports
- Supports Philips standard Inter-IC Sound (I²S) bus for external digital audio chip interface at 44.1 kHz and 48 kHz

- AC97 Host Controller mode with support for 2 audio channels supporting fixed rate transfers with a 48 kHz sampling rate.
- Used together with the Digital Audio Mux (AUDMUX) module to provide flexible audio and voice routing options

2.5 Display and Video Modules

There are two separate LCD controllers in the i.MX21S processor—the LCDC and SLCDC that support both dumb and smart LCD panels. A dumb LCD panel has no built-in memory and requires an external controller to send display data at a fixed rate. Such panels typically support high refresh rates suitable for graphics, games, and video applications. The LCD controller in the i.MX21S processor is an AHB master and can transfer display data from system memory (SDRAM).

Smart panels have built-in memory and a display controller. An advantage of the built-in memory and controller, is that the refresh function is done by the local LCD controller and only data that is changing must be updated thus offering a reduced transfer rate and lower power operation.

Both LCD controllers in the i.MX21S processor provide glueless connection to external gray-scale or color LCD panels.

2.5.1 LCD Controller (LCDC)

The LCDC features include the following:

- Software programmable screen size (up to 800 × 600) to support single (non-split) monochrome, color STN panels and color TFT panels
- Support color depth for CSTN panels: 4- or 8-bit mapping from 256 × 18 table, 12-bit true color
- Support color depth for TFT panels: 4- or 8-bit mapping from 256 × 18 table, 16-bit/18-bit/24-bit true color
- Up to 16 grey levels out of 16 palettes
- Capable of directly driving popular LCD drivers from manufacturers including Motorola, Sharp, Hitachi, and Toshiba
- Support for data bus width of 16-bit or 18-bit TFT panels
- Support for data bus width of 8-bit, 4-bit, 2-bit, and 1-bit monochrome LCD panels
- Direct interface to Sharp[®] 320 × 240 and 240 × 320 HR-TFT panels and other generic panels
- Support for logical operation between color hardware cursor and background
- LCD contrast control using 8-bit PWM
- Support for self-refresh LCD modules
- Hardware panning (soft horizontal scrolling)
- Windowing support for one graphic or text overlay

2.5.2 Smart LCD Controller (SLCDC)

The SLCDC transparently and efficiently transfers image data from system memory to an external LCD controller. The SLCDC module contains a DMA controller that transfers image and control data from system memory to the SLCDC FIFO where it is formatted and sent out to the external LCD controller.

The SLCDC can be configured to write image data to an external LCD controller via a 4-line serial, 3-line serial, an 8- or 16-bit parallel interface. The SLCDC has two FIFOs where command and display data are loaded via DMA. The display data is tagged with commands that are used by the SLCDC to communicate display information and data to the Smart LCD panel.

The command tagged data format of the SLCDC provides flexibility and ease of connection to existing and new smart LCD panels.

2.6 Two Multimedia Card and Secure Digital Host Controller Modules

The Multimedia Card/Secure Digital Host module (MMC/SD) integrates MMC support with SD memory and I/O functions. The features include:

- Fully compatible with the MMC system specification version 2.2
- Fully compatible with the SD Memory Card specification 1.0 and SD I/O specification 1.0 with 1 and 4 channel(s)
- Up to ten MMC cards and one SD supported by standard (maximum data rate with up to ten cards)
- Supports hot swappable operation
- Data rates from 25 Mbps to 100 Mbps
- Dedicated power pin
- Part of the External Memory Interface (EMI) complex comprising the Nand Flash Controller, Wireless External Interface to Memory (WEIM) and SDRAM Controller

2.7 Digital Audio Mux

The Digital Audio Mux (AUDMUX) provides a programmable interconnect fabric for voice, audio and synchronous data routing between the i.MX21S processor's SSI modules and external SSI, audio and voice codecs. The AUDMUX features include:

- Supports 1 host and 3 peripheral interfaces
- Flexible audio, voice and data routing without host processor intervention
- Built-in support for network mode connection of host and peripheral interfaces
- Separate and simultaneous audio paths from hosts to peripherals
- External 4-wire connection to synchronous devices, audio and voice codecs

2.8 Connectivity and Expansion

There are multiple peripheral modules in the i.MX21S processor that provide external connection capability. All peripherals that have FIFOs support DMA transfers to and from the FIFOs. This minimizes

CPU intervention and reduces interrupt overhead to the system. The exception to this is the Pulse Width Modulator that includes FIFOs, however, does not support DMA.

2.8.1 Three Universal Asynchronous Receiver/Transmitters (UART1, UART3, and UART4)

The UART modules are capable of standard RS-232 non-return-to-zero (NRZ) encoding format and IrDA-compatible infrared modes. Each UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility to the i.MX21S processor. Features include:

- Supports serial data transmit/receive operation: 7 or 8 data bits, 1 or 2 stop bits, programmable parity (even, odd, or none)
- Programmable baud rates
- Automatic baud rate detection
- 32-bytes FIFO for transmit and 32 half-words FIFO for receive data
- IrDA Serial Infra-Red (SIR) mode support

2.8.2 USB On-The-Go (USB OTG) Controller

The USB controller in the i.MX21S processor implements the USB On-The-Go (USB OTG) supplement. The USB OTG module is compliant to the USB 2.0 and operates at full and low speeds as specified in USB 2.0. The OTG port is capable of connecting to a USB host or client device and uses the Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) to switch between Host and Function roles. One of the dual host ports is dedicated for connection to a smartphone USB client device and the other host port is available for connection to other client devices. The connection to the smartphone forms the interprocessor link as an alternate to a UART-based link.

Built-in switching logic implements a bypass mode in which the internal host port is bypassed to allow an external USB host and the smartphone USB client to be directly connected. This feature enables the external USB host to directly control the smartphone modem for debug or for production programming. [Figure 2](#) shows the USB OTG block.

The USB OTG module is a bus master and takes ownership of the bus for DMA. This allows the USB OTG to continue operation while the CPU is in a low power mode.

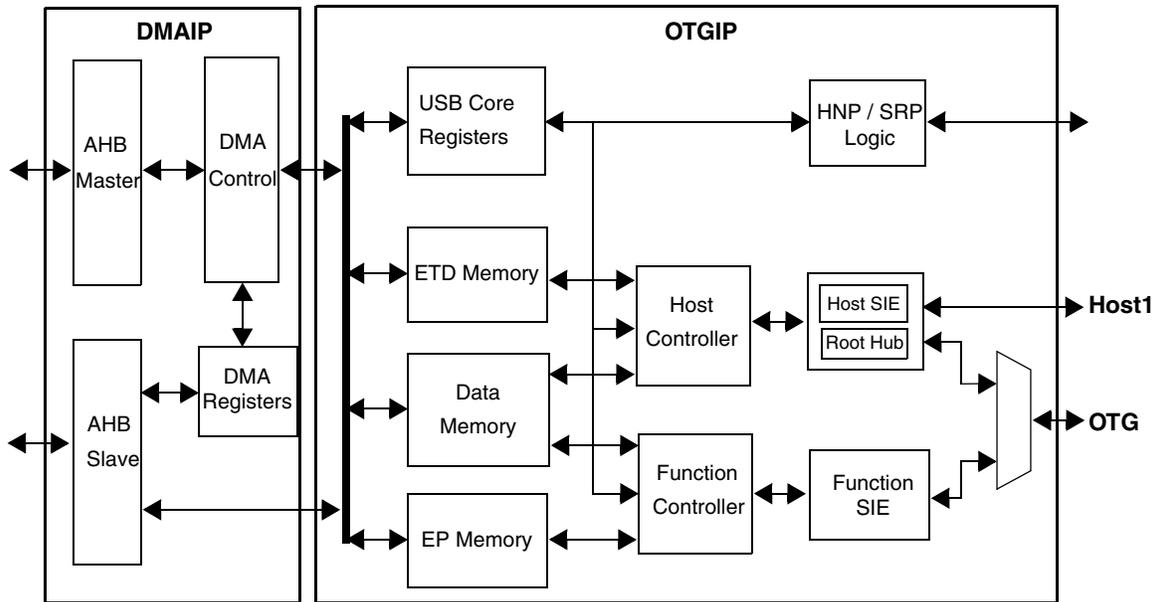


Figure 2. i.MX21S USB On-The-Go Controller Block Diagram

- Compliant with the USB 2.0 specification for operation at full speed (12 Mbit/sec) and low speed (1.5 Mbit/sec)
- Fully compliant with the USB On-The-Go specification
- Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) implemented in hardware and can also be controlled by software
- Transaction scheduling and transfer level protocol implemented in hardware including bandwidth management, data toggle and retry
- AMBA AHB 2.0 Bus Master DMA Controller:
 - 32 DMA Channels for Host Controller EndPoint Transfer Descriptors
 - 32 DMA Channels for Function Controller EndPoint Descriptors
- USB function supports 32 physical endpoints:
 - 16 IN endpoints and 16 OUT endpoints
 - Programmable for type (control, interrupt, bulk, isochronous), packet size, and buffering
- Double buffering support for all four types of Host and Function controller transactions
- Separate descriptor and data memory space
- Direct device-to-device transfers in one frame
- Power savings mode for Host Controller and suspend mode for Function Controller
- The USB Host port 1 supports external transceiver bypass mode

2.9 Debug Capability

The i.MX21S processor offers designers and programmers with full-debug capabilities through industry-standard JTAG interface and the ability to bootload using either a serial or USB interface.

- UART Bootstrap mode function:
 - Allows system initialization and program or data download to system memory via USB or UART1
 - Accepts execution command to run program stored in system memory
 - Supports memory/register read/write operation of selectable data size of byte, half-word, or word
 - Provides a 16-byte instruction buffer for ARM instruction storage and execution
- USB Bootstrap mode function
 - Supports bootstrapping through USB OTG port
- JTAG port to support generic ARM debug tools

2.9.1 PCMCIA/CF Interface

The PCMCIA/CF host controller module provides all the control logic for a PCMCIA socket interface and requires only additional external analog power switching logic and buffering. The controller supports one PCMCIA socket and includes the following features:

- PCMCIA/CF host controller interface compliant with the PCMCIA standard release 2.1 (for I/O Cards) and fully compliant with the Compact Flash Specification V1.4
- Supports one PCMCIA or CF socket
- Supports hot-insertion, card detection and removal
- Mapping to common memory space, attribute memory space and I/O space.
- Supports 5 programmable memory and IO windows.
- Generates a single interrupt to the CPU
- Programmable card access timing to interface with slower devices
- Supports TrueIDE mode
- Provides special control signals for external buffering to separate high and low speed paths

2.9.2 Keypad Port

The Keypad Port is a 16-bit peripheral which can be used either for keypad matrix scanning or as general purpose I/O. Features include:

- Supports up to 8 × 8 external key pad matrix
- Open drain design
- Glitch suppression circuit prevents erroneous key detection
- Multiple keys detection
- Standby key press detection

2.9.3 Fast Infra-Red Interface (FIRI)

The Fast Infra-Red Interface (USB device module) in the i.MX21S processor implements both the Medium Infra-Red (MIR) and Fast Infra-Red (FIR) protocols. In MIR mode, the FIRI supports wireless

communications at 0.576 Mbps and 1.152 Mbps and uses a framed transmission protocol which follows the High-Level Data Link Controller (HDLC) protocol. In FIR mode, the module operates at 4 Mbps with 4 Pulse Position Modulation (4PPM) defined by IrDA, version 1.4.

In addition to the MIR and FIR modes, the i.MX21S processor supports SIR protocol on all of the UART modules. Only UART1 may be used together with the FIRI as these two modules share their pins for transparent speed and protocol stepping from SIR to MIR or SIR to FIR modes.

Figure 3 shows the FIRI sharing pins with the UART module and pin selection is controlled via GPIO configuration.

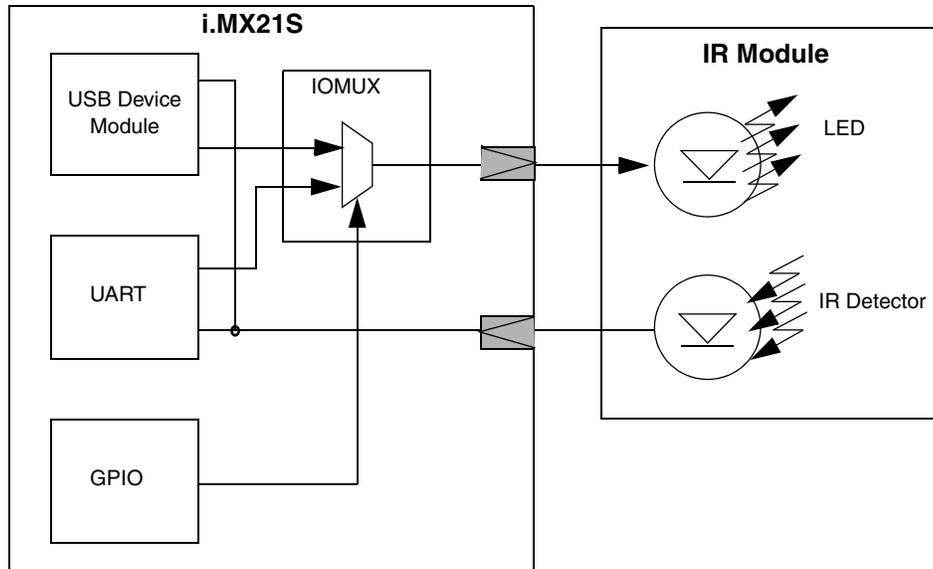


Figure 3. Fast Infra-Red Interface

The USB device module can be divided to the following functional parts:

- Packet assembler
- Searcher
- 4PPM modulator/demodulator
- CRC32 encoder and decoder
- DMA capable receive and transmit FIFOs

2.9.4 1-Wire[®] Interface

The 1-Wire module is a peripheral device that communicates with the ARM926EJ-S Core and provides a communication line to a 1 Kbit Add-Only Memory (DS2502). The 1-Wire interface features include:

- Supports 1-Wire interface to a 1Kbit Add-Only Memory (DS2502)
- Implements 1-Wire protocol defined by Dallas Semiconductors

2.10 Power Management

The i.MX21S processor's power management features are as follows:

- Support for 3 power modes of operation: RUN, DOZE, and STOP
- Aggressive clock gating within modules
- Active well biasing technique to reduce standby mode current consumption

2.11 Electronic and Package Information

The i.MX21S processor features the following electronic and package information:

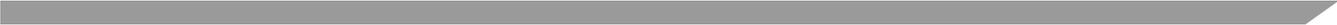
- Operating voltage
 - I/O voltage: 1.7 V to 3.3 V
 - Internal logic voltage: 1.45 V to 1.65 V
- Package
 - Type: 0.65 mm and 0.8 mm pitch MAPBGA
 - Dimensions: 14mm × 14mm and 17mm × 17mm
 - Pins: 289

3 Document Revision History

Table 1 provides the changed information for the Rev. 1.2 release of this document.

Table 1. Document Revision History

Location	Description of Change
Section 2.4.3, "Two Synchronous Serial Interfaces with Inter-IC Sound (I2S) and AC97 Host Controller Module (SSI/I2S/AC97)	Removed reference to AC97 supporting variable mode.
Was Section 2.5, Peripheral Support	Removed reference to CMOS Sensor Interface.



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