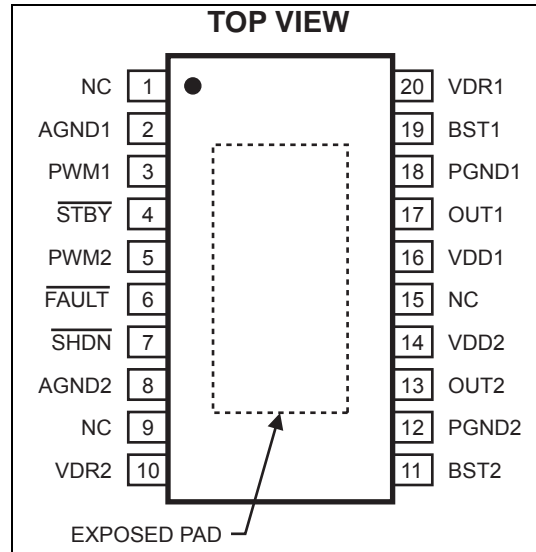


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T _A)
MP8042DF	TSSOP20F	MP8042DF	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP8042DF–Z).
 For RoHS compliant packaging, add suffix –LF (e.g. MP8042DF–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

VDD1/2 Supply Voltage	26V
OUT1/2 Pin Voltage	–0.3V to V _{DD} + 0.3V
OUT1/2 to BST1/2	–0.3V to +6V
Voltage at All Other Pins	–0.3V to +6V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	3.1W
Storage Temperature	–55°C to +150°C
Junction Temperature	150°C
Lead Temperature	260°C

Recommended Operating Conditions ⁽³⁾

VDD1/2 Supply Voltage	7.5V to 24V
Peak Output Current	5A Maximum
Operating Junct. Temp (T _J)	–40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
TSSOP20F	40	6

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)–T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

$V_{DD1} = V_{DD2} = 12V$, $V_{SHDN} = 5V$, $T_A = +25^\circ C$, unless otherwise specified.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VDD Operating Current		$I_{LOAD} = 0A$		2.1	2.5	mA
VDD Shutdown Current		$V_{SHDN} = 0V$		4.0	10	μA
VDD Operating Threshold, Low			5.8	6.1		V
VDD Operating Threshold, High				6.63	7.2	V
\overline{STBY} Threshold, Low			1.0	1.2		V
\overline{STBY} Threshold, High				1.85	2.0	V
\overline{SHDN} Threshold, Low			1.0	1.2		V
\overline{SHDN} Threshold, High				1.9	2.0	V
PWM _{1,2} Threshold, Low			1.5	1.69		V
PWM _{1,2} Threshold, High				1.83	2.0	V
PWM Input Bias Current				1		μA
OUT On Resistance ⁽⁵⁾		$V_{DD} = 7.5V$, High-Side and Low-Side		0.15		Ω
OUT Current Limit ⁽⁵⁾		$V_{PWM} = 5$, Sinking		5		A
		$V_{PWM} = 0$, Sourcing		5		A
OUT Switching Frequency		$V_{PWM} = 0$ to 2V, 50% Duty Cycle			0.6	MHz
OUT Maximum Duty Cycle ⁽⁶⁾		$V_{DD} = 7.5V$, $V_{PWM} = 2V$, $C_{BST} = 100nF$, $f_{SW} = 3.3kHz$		99.5		%
OUT Rise/Fall Time ⁽⁵⁾		$V_{PWM} = 0V$ to 5V		10		ns
PWM Pulse Width		$V_{PWM} = 0V$ to 2V, High or Low Pulse		200		ns
Dead Time ⁽⁵⁾		$I_{OUT} = \pm 100mA$		30		ns
PWM to OUT Delay Time Rising		$V_{PWM} = 0V$ to 5V		37	45	ns
PWM to OUT Delay Time Falling		$V_{PWM} = 5$ to 0V		54	65	ns
Thermal Shutdown Temperature ⁽⁵⁾		T_J Rising, Hysteresis = 20°C		150		°C

Notes:

5) Not production tested.

6) OUT drives low for 1.5 μs every 300 μs to charge the BST to SW capacitor.

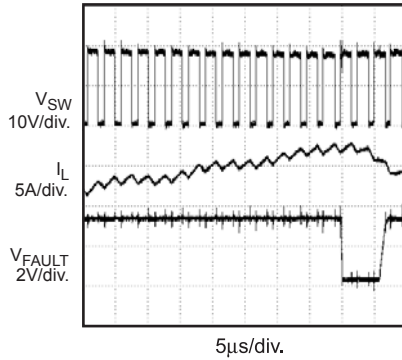
PIN FUNCTIONS

Pin #	Name	Description
1	NC	No Connect.
2	AGND1	Analog Ground 1.
3	PWM1	Driver Logic Input 1. Drive PWM1 with the signal that controls the MP8042 OUT1. Drive PWM high to turn on the high side switch; drive PWM low to turn on the low-side switch.
4	$\overline{\text{STBY}}$	Standby Input. Default low (internal pull-down). If driven high, the output of drivers is determined by the PWM1/2. If driven low, the output of both drivers is high impedance.
5	PWM2	Driver Logic Input 2. Drive PWM2 with the signal that controls the MP8042 OUT2. Drive PWM high to turn on the high-side switch; drive PWM low to turn on the low-side switch.
6	$\overline{\text{FAULT}}$	Fault Output. A low output at $\overline{\text{FAULT}}$ indicates that the MP8042 has detected an over temperature or over current condition. This output is open drain.
7	$\overline{\text{SHDN}}$	Shutdown Input. When low, both channels will be shut off.
8	AGND2	Analog Ground 2.
9	NC	No Connect.
10	VDR2	Gate Drive Supply Bypass 2. The voltage at VDR2 is supplied from an internal regulator from VDD2. VDR2 powers the internal circuitry and internal MOSFET gate drive for the OUT2 stage. Bypass VDR2 to PGND with a 0.1 μ F to 10 μ F capacitor.
11	BST2	Bootstrap Supply 2. BST2 powers the high-side gate of the OUT2 stage. Connect a 0.1 μ F or greater capacitor between BST2 and OUT2.
12	PGND2	Power Ground 2. Connect the exposed pad on bottom side to the ground plane.
13	OUT2	Switched Output 2. Connect the output LC filter to OUT2. OUT2 is valid approximately 100 μ s after VDD2 goes high.
14	VDD2	Power Supply Input 2. Connect VDD2 to the positive side of the input power supply. Bypass VDD2 to PGND as close to the IC as possible.
15	NC	No Connect.
16	VDD1	Power Supply Input 1. Connect VDD1 to the positive side of the input power supply. Bypass VDD1 to PGND as close to the IC as possible.
17	OUT1	Switched Output 1. Connect the output LC filter to OUT1. OUT1 is valid approximately 100 μ s after VDD1 goes high.
18	PGND1	Power Ground 1. Connect the exposed pad on bottom side to the ground plane.
19	BST1	Bootstrap Supply 1. BST1 powers the high-side gate of the OUT1 stage. Connect a 0.1 μ F or greater capacitor between BST1 and OUT1.
20	VDR1	Gate Drive Supply Bypass 1. The voltage at VDR1 is supplied from an internal regulator from VDD1. VDR1 powers the internal circuitry and internal MOSFET gate drive for the OUT1 stage. Bypass VDR1 to PGND with a 0.1 μ F to 10 μ F capacitor.

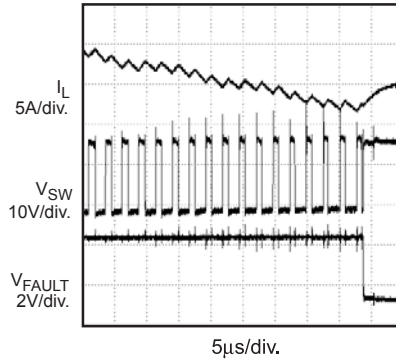
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD1} = V_{DD2} = 20V$, $V_{SHDN} = 5V$, $T_A = +25^\circ C$, unless otherwise specified.

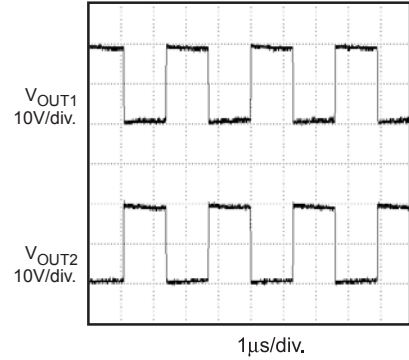
Short Circuit Positive Current



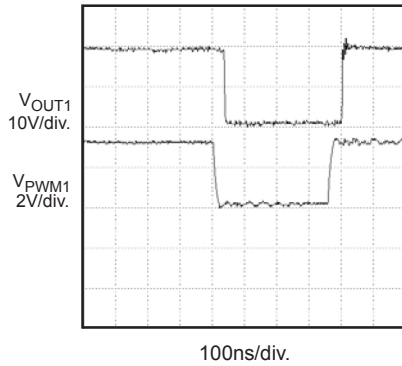
Short Circuit Negative Current



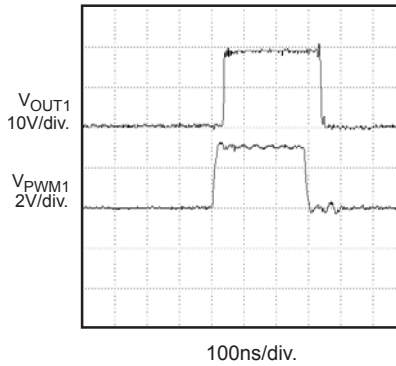
Normal Switch Waveform



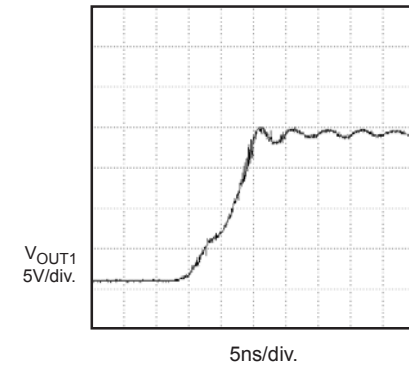
Input/Output Waveform Negative Pulse



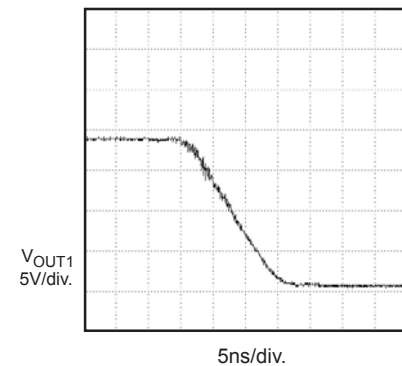
Input/Output Waveform Positive Pulse



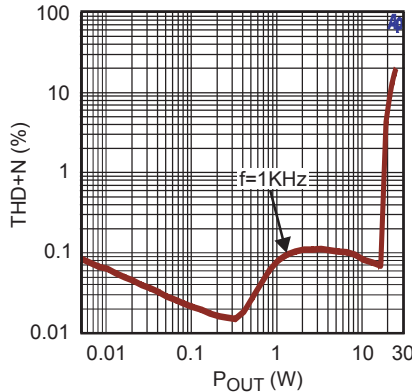
Output Rise-Time



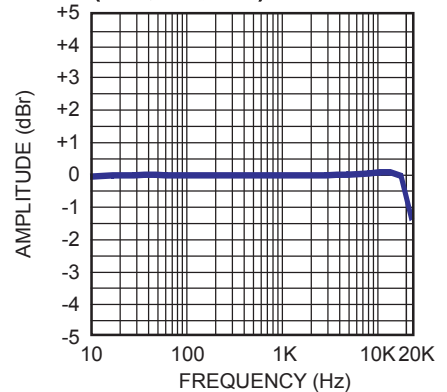
Output Fall-Time



THD+N vs. P_OUT (19V, 8Ω)



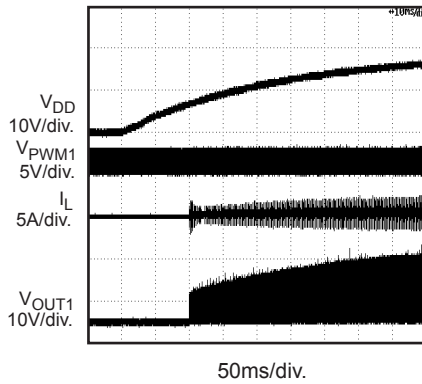
Frequency Response (19V, 8Ω, 1W)



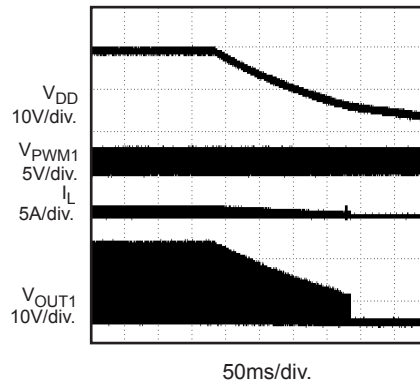
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{DD1} = V_{DD2} = 20V$, $V_{SHDN} = 5V$, $T_A = +25^\circ C$, unless otherwise specified.

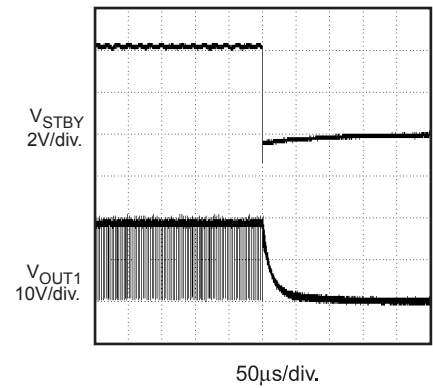
Start-up



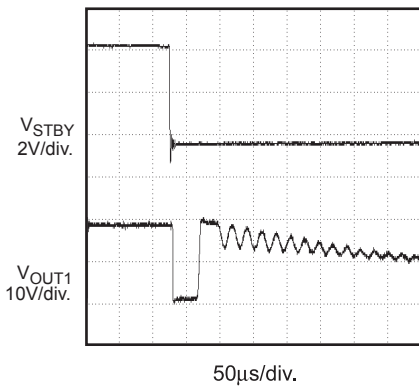
Shut-down



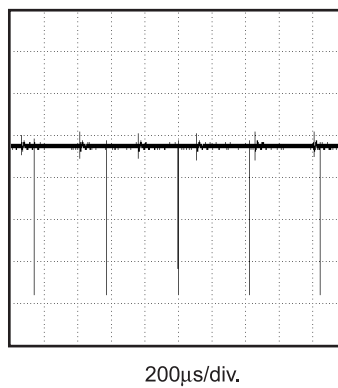
Standby



Standby



BS Recharge Cycling
($V_{DD} = 19V$, $R_L = 16\Omega$)



OPERATION

The MP8042 is a high voltage, dual channel power half-bridge that can be configured as the output of a Class D amplifier. The output is in phase with the input, and the dead time is optimized for symmetrical performance, regardless of load conditions.

When shutdown pin ($\overline{\text{SHDN}}$) is low, both channels 1 and 2 will be shut off. When the standby pin ($\overline{\text{STBY}}$) is pulled low, it causes the outputs of both channels to go into high impedance. However, when the voltage across the BST1/2 and OUT1/2 pins drops sufficiently low, the bottom MOSFET is turned on to refresh the external bootstrap capacitor. For a bootstrap capacitor of 100nF, the refresh time is approximately 300ns.

In order to prevent erratic operation, two under voltage lockout (UVLO) circuits are used. One of them is to ensure that the supply for the bottom gate drive circuit is sufficiently high and the other is for the top gate driver.

Fault Protection

To protect the power MOSFETs, two layers of protection are provided. The first is the current limit, wherein if the current through either the top or the bottom MOSFET exceeds an internally preset value of 5A, that particular MOSFET is immediately shut down and the complementary MOSFET is turned on. If this fails to reset the current and there is an indication that the current is going to runaway, the current foldback will kick in. This ensures that the current is reset close to zero before resuming operation.

Thermal monitoring is also integrated into the MP8042. If the die temperature rises above 150°C, both switches are turned off. The temperature must fall below 130°C before normal operation resumes.

To enhance the robustness of the device under short circuit condition, a capacitor can be connected to the $\overline{\text{FAULT}}$ pin, as shown in figure 1. The time constant of the RC is selected to be greater than 50ms for the $\overline{\text{FAULT}}$ node to reach 1V. Under short circuit condition, the $\overline{\text{FAULT}}$ node will be reset to zero and the part will be placed in standby mode until the voltage at the $\overline{\text{STBY}}$ pin is above 1V.

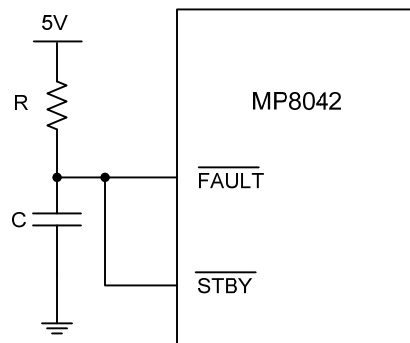


Figure 1— Fault Protection Circuit

Fault Output

The MP8042 includes an open drain, active low fault indicator output ($\overline{\text{FAULT}}$). A fault will be indicated if the current limit is tripped or the thermal shutdown is tripped.

A fault on any channel causes the $\overline{\text{FAULT}}$ pin to be pulled low. However, only that fault channel has its output set to high impedance.

Do not apply more than 6V to the $\overline{\text{FAULT}}$ pin.

BLOCK DIAGRAM

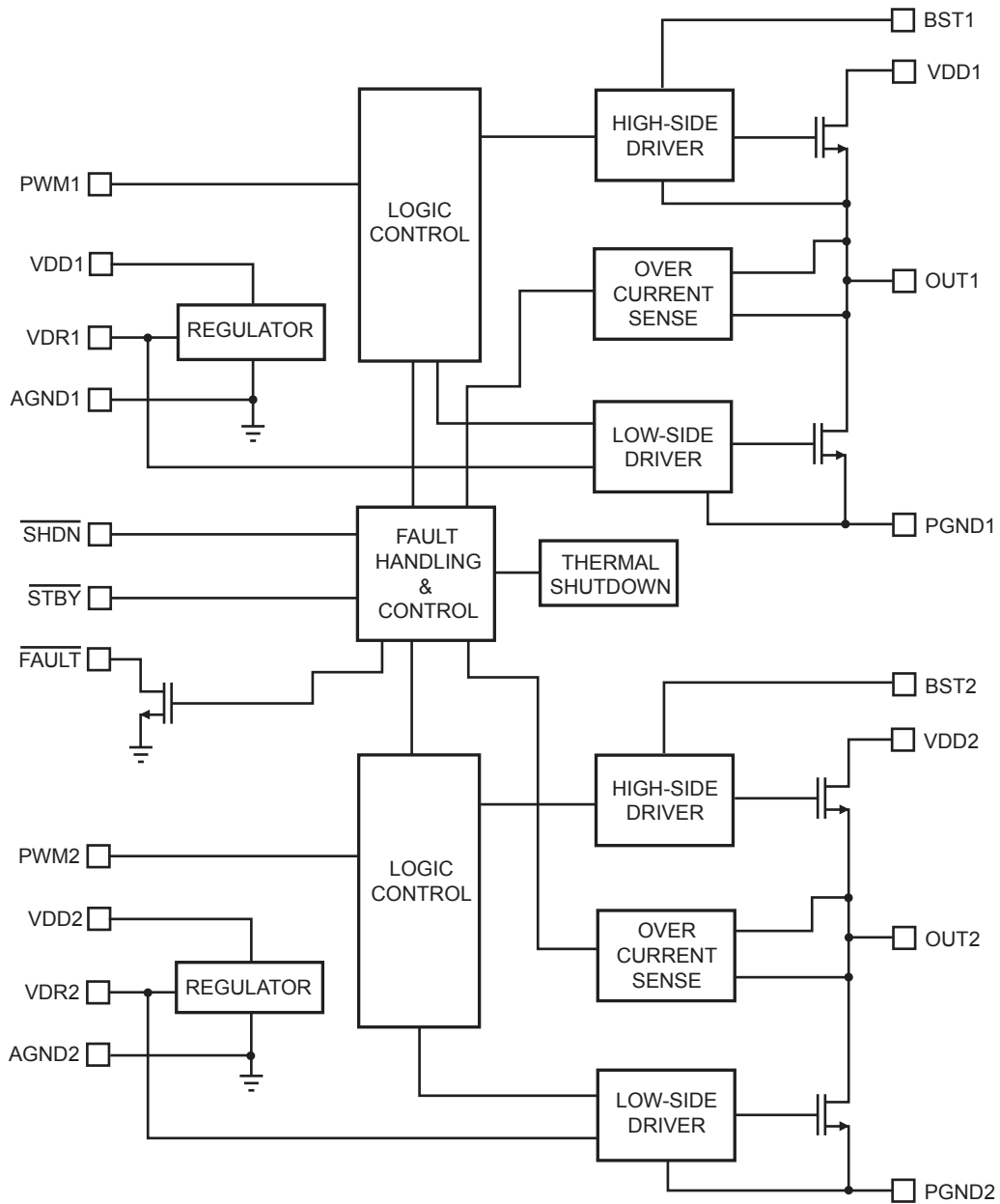
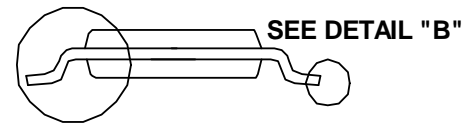
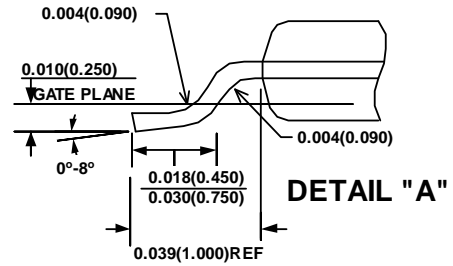
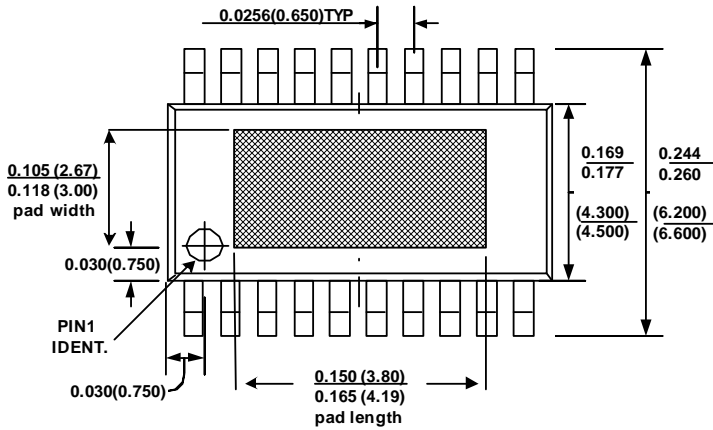


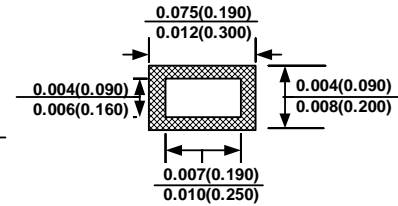
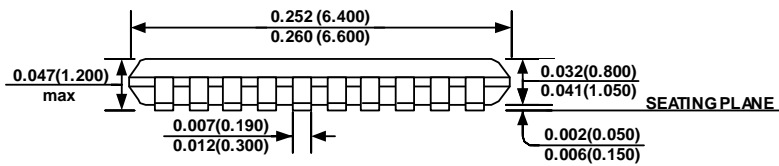
Figure 2—Function Block Diagram

PACKAGE INFORMATION

TSSOP20F



SEE DETAIL "A"



NOTE:
1) Control dimension is in inches. Dimension in bracket is millimeters.

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