

## FEATURES

- Overvoltage protection up to  $-55$  V and  $+55$  V
- Power-off protection up to  $-55$  V and  $+55$  V
- Overvoltage detection on source pins
- Low on resistance: 10  $\Omega$
- On-resistance flatness: 0.5  $\Omega$
- 5.5 kV human body model (HBM) ESD rating
- Latch-up immune under any circumstance
- Known state without digital inputs present

## ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

## APPLICATIONS

- Avionics
- Analog input/output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation
- Automatic test equipment
- Communication systems
- Relay replacement

## GENERAL DESCRIPTION

The **ADG5412F-EP** contains four independently controlled single-pole/single-throw (SPST) switches. The **ADG5412F-EP** has four switches that turn on with Logic 1 inputs. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. The digital inputs are compatible with 3 V logic inputs over the full operating supply range.

When no power supplies are present, the switch remains in the off condition, and the switch inputs are high impedance. Under normal operating conditions, if the analog input signal levels on any  $S_x$  pin exceed  $V_{DD}$  or  $V_{SS}$  by a threshold voltage,  $V_T$ , the switch turns off. Input signal levels up to  $+55$  V or  $-55$  V relative to ground are blocked, in both the powered and unpowered condition.

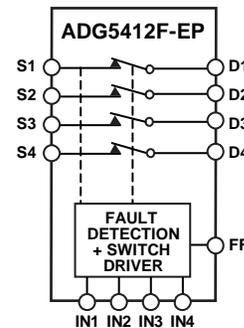
The low on resistance of these switches, combined with on-resistance flatness over a significant portion of the signal range make them an ideal solution for data acquisition and gain

Rev. A

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## FUNCTIONAL BLOCK DIAGRAM



NOTES  
1. SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 1.

12706-001

switching applications where excellent linearity and low distortion are critical.

## PRODUCT HIGHLIGHTS

1. Source pins are protected against voltages greater than the supply rails, up to  $-55$  V and  $+55$  V.
2. Source pins are protected against voltages between  $-55$  V and  $+55$  V in an unpowered state.
3. Overvoltage detection with digital output indicates operating state of switches.
4. Trench isolation guards against latch-up.
5. Optimized for low on resistance and on-resistance flatness.
6. The **ADG5412F-EP** can be operated from a dual supply of  $\pm 5$  V up to  $\pm 22$  V or a single power supply of  $+8$  V up to  $+44$  V.

Additional application and technical information can be found in the [ADG5412F](#) data sheet.

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**REVISION HISTORY**

**8/15—Rev. 0 to Rev. A**

Changes to Features Section.....	1
Added Enhanced Product Features Section.....	1

**7/15—Revision 0: Initial Version**

## SPECIFICATIONS

## ±15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $C_{DECOUPLING} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.

Table 1.

Parameter	+25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	$V_{DD} = 13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$ , see Figure 30
On Resistance, $R_{ON}$	10			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	11.2	14	16.5	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	9.5			$\Omega$ typ	$V_S = \pm 9\text{ V}$ , $I_S = -10\text{ mA}$
	10.7	13.5	16	$\Omega$ max	
	0.05			$\Omega$ typ	
	0.5	0.6	0.7	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	0.05			$\Omega$ typ	$V_S = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$
	0.35	0.5	0.5	$\Omega$ max	
	0.6			$\Omega$ typ	
	0.9	1.1	1.1	$\Omega$ max	
Threshold Voltage, $V_T$	0.1			$\Omega$ typ	$V_S = \pm 9\text{ V}$ , $I_S = -10\text{ mA}$
	0.4	0.5	0.5	$\Omega$ max	
	0.7			V typ	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ , see Figure 31
	$\pm 1.5$	$\pm 5.0$	$\pm 21.0$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S = \pm 10\text{ V}$ , $V_D = \mp 10\text{ V}$ , see Figure 31
	$\pm 1.5$	$\pm 5.0$	$\pm 18.0$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.3$			nA typ	$V_S = V_D = \pm 10\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 2.0$	$\pm 4.5$	nA max	
<b>FAULT</b>					
Source Leakage Current, $I_S$ With Overvoltage			$\pm 78$	$\mu\text{A}$ typ	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = 16.5\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 35
Power Supplies Grounded or Floating			$\pm 40$	$\mu\text{A}$ typ	
Drain Leakage Current, $I_D$ With Overvoltage	$\pm 2.0$			nA typ	$V_{DD} = 16.5\text{ V}$ , $V_{SS} = 16.5\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 35
Power Supplies Grounded	$\pm 8.0$ $\pm 10$	$\pm 15.0$	$\pm 49.0$	nA max nA typ	
Power Supplies Floating	$\pm 30$ $\pm 10$	$\pm 50$ $\pm 10$	$\pm 100$ $\pm 10$	nA max $\mu\text{A}$ typ	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $I_{NX} = 0\text{ V}$ , see Figure 36
<b>DIGITAL INPUTS/OUTPUTS</b>					
Input Voltage High, $V_{INH}$			2.0	V min	$V_{IN} = V_{GND}$ or $V_{DD}$
Input Voltage Low, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	$\pm 0.7$			$\mu\text{A}$ typ	
			$\pm 1.2$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	5.0			pF typ	
Output Voltage High, $V_{OH}$	2.0			V min	
Output Voltage Low, $V_{OL}$	0.8			V max	

Parameter	+25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
t <sub>ON</sub>	400			ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
	495	525	550	ns max	V <sub>S</sub> = 10 V, see Figure 44
t <sub>OFF</sub>	410			ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
	510	545	555	ns max	V <sub>S</sub> = 10 V, see Figure 44
Overvoltage Response Time, t <sub>RESPONSE</sub>	460			ns min	V <sub>S1</sub> = V <sub>S2</sub> = 10 V, see Figure 44
	585	615	630	ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 2 pF, see Figure 39
Overvoltage Recovery Time, t <sub>RECOVERY</sub>	720			ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 2 pF, see Figure 40
	930	1050	1100	ns max	
Interrupt Flag Response Time, t <sub>DIGRESP</sub>	85		115	ns typ	C <sub>L</sub> = 10 pF, see Figure 41
Interrupt Flag Recovery Time, t <sub>DIGREC</sub>	60		85	μs typ	C <sub>L</sub> = 10 pF, see Figure 42
	600			ns typ	C <sub>L</sub> = 10 pF, R <sub>PULLUP</sub> = 1 kΩ, see Figure 43
Charge Injection, Q <sub>INJ</sub>	680			pC typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF, see Figure 45
Off Isolation	-70			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 33
Channel-to-Channel Crosstalk	-90			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 34
Total Harmonic Distortion Plus Noise, THD + N	0.0015			% typ	R <sub>L</sub> = 10 kΩ, V <sub>S</sub> = 15 V p-p, f = 20 Hz to 20 kHz, see Figure 38
-3 dB Bandwidth	270			MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, see Figure 37
Insertion Loss	-0.72			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 37
C <sub>S</sub> (Off)	13			pF typ	V <sub>S</sub> = 0 V, f = 1 MHz
C <sub>D</sub> (Off)	12			pF typ	V <sub>S</sub> = 0 V, f = 1 MHz
C <sub>D</sub> (On), C <sub>S</sub> (On)	24			pF typ	V <sub>S</sub> = 0 V, f = 1 MHz
<b>POWER REQUIREMENTS</b>					
Normal Mode					V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = -16.5 V, GND = 0 V, digital inputs = 0 V, 5 V, or V <sub>DD</sub>
I <sub>DD</sub>	0.9			mA typ	
	1.2		1.3	mA max	
I <sub>GND</sub>	0.4			mA typ	
	0.55		0.6	mA max	
I <sub>SS</sub>	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					V <sub>S</sub> = ±55 V
I <sub>DD</sub>	1.2			mA typ	
	1.6		1.8	mA max	
I <sub>GND</sub>	0.8			mA typ	
	1.0		1.1	mA max	
I <sub>SS</sub>	0.5			mA typ	
	1.0		1.8	mA max	
V <sub>DD</sub> /V <sub>SS</sub>			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

**±20 V DUAL SUPPLY**

$V_{DD} = 20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ ,  $C_{DECOUPLING} = 0.1\ \mu\text{F}$ , unless otherwise noted.

**Table 2.**

Parameter	+25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	$V_{DD} = 18\text{ V}$ , $V_{SS} = -18\text{ V}$ , see Figure 30
On Resistance, $R_{ON}$	10			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
	11.5	14.5	16.5	$\Omega$ max	
	9.5			$\Omega$ typ	$V_S = \pm 13.5\text{ V}$ , $I_S = -10\text{ mA}$
	11	14	16.5	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.05			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
	0.35	0.5	0.5	$\Omega$ max	
	0.05			$\Omega$ typ	$V_S = \pm 13.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.35	0.5	0.5	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.0			$\Omega$ typ	$V_S = \pm 15\text{ V}$ , $I_S = -10\text{ mA}$
	1.4	1.5	1.5	$\Omega$ max	
	0.1			$\Omega$ typ	$V_S = \pm 13.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.4	0.5	0.5	$\Omega$ max	
Threshold Voltage, $V_T$	0.7			V typ	See Figure 26
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 22\text{ V}$ , $V_{SS} = -22\text{ V}$
	$\pm 1.5$	$\pm 5.0$	$\pm 21.0$	nA max	$V_S = \pm 15\text{ V}$ , $V_D = \mp 15\text{ V}$ , see Figure 31
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S = \pm 15\text{ V}$ , $V_D = \mp 15\text{ V}$ , see Figure 31
	$\pm 1.5$	$\pm 5.0$	$\pm 18.0$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.3$			nA typ	$V_S = V_D = \pm 15\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 2.0$	$\pm 4.5$	nA max	
<b>FAULT</b>					
Source Leakage Current, $I_S$ With Overvoltage			$\pm 78$	$\mu\text{A}$ typ	$V_{DD} = 22\text{ V}$ , $V_{SS} = -22\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 35
Power Supplies Grounded or Floating			$\pm 40$	$\mu\text{A}$ typ	$V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $INx = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$ , see Figure 36
Drain Leakage Current, $I_D$ With Overvoltage	$\pm 5.0$			nA typ	$V_{DD} = +22\text{ V}$ , $V_{SS} = -22\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 35
	$\pm 1.0$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$ max	
Power Supplies Grounded	$\pm 10$			nA typ	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $INx = 0\text{ V}$ , see Figure 36
	$\pm 30$	$\pm 50$	$\pm 100$	nA max	
Power Supplies Floating	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ typ	$V_{DD} = \text{floating}$ , $V_{SS} = \text{floating}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $INx = 0\text{ V}$ , see Figure 36
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2.0	V min	
Input Voltage Low, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.7			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			1.2	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	5.0			pF typ	
Output Voltage High, $V_{OH}$	2.0			V min	
Output Voltage Low, $V_{OL}$	0.8			V max	

Parameter	+25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
t <sub>ON</sub>	400			ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
	500	530	555	ns max	V <sub>S</sub> = 10 V, see Figure 44
t <sub>OFF</sub>	415			ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
	515	550	565	ns max	V <sub>S</sub> = 10 V, see Figure 44
Overvoltage Response Time, t <sub>RESPONSE</sub>	370			ns min	V <sub>S1</sub> = V <sub>S2</sub> = 10 V, see Figure 44
	480	500	515	ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 2 pF, see Figure 39
Overvoltage Recovery Time, t <sub>RECOVERY</sub>	840			ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 2 pF, see Figure 40
	1200	1400	1700	ns max	
Interrupt Flag Response Time, t <sub>DIGRESP</sub>	85		115	ns typ	C <sub>L</sub> = 10 pF, see Figure 41
Interrupt Flag Recovery Time, t <sub>DIGREC</sub>	60		85	μs typ	C <sub>L</sub> = 10 pF, see Figure 42
Charge Injection, Q <sub>INJ</sub>	600			ns typ	C <sub>L</sub> = 10 pF, R <sub>PULLUP</sub> = 1 kΩ, see Figure 43
Off Isolation	640			pC typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF, see Figure 45
Channel-to-Channel Crosstalk	-70			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 33
Total Harmonic Distortion Plus Noise, THD + N	-90			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 34
-3 dB Bandwidth	0.001			% typ	R <sub>L</sub> = 10 kΩ, V <sub>S</sub> = 20 V p-p, f = 20 Hz to 20 kHz, see Figure 38
Insertion Loss	270			MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, see Figure 37
	-0.73			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 37
C <sub>S</sub> (Off)	12			pF typ	V <sub>S</sub> = 0 V, f = 1 MHz
C <sub>D</sub> (Off)	11			pF typ	V <sub>S</sub> = 0 V, f = 1 MHz
C <sub>D</sub> (On), C <sub>S</sub> (On)	23			pF typ	V <sub>S</sub> = 0 V, f = 1 MHz
<b>POWER REQUIREMENTS</b>					
V <sub>DD</sub> = 22 V, V <sub>SS</sub> = -22 V, digital inputs = 0 V, 5 V, or V <sub>DD</sub>					
Normal Mode					
I <sub>DD</sub>	0.9			mA typ	
	1.2		1.3	mA max	
I <sub>GND</sub>	0.4			mA typ	
	0.55		0.6	mA max	
I <sub>SS</sub>	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					V <sub>S</sub> = ±55 V
I <sub>DD</sub>	1.2			mA typ	
	1.6		1.8	mA max	
I <sub>GND</sub>	0.8			mA typ	
	1.0		1.1	mA max	
I <sub>SS</sub>	0.5			mA typ	
	1.0		1.8	mA max	
V <sub>DD</sub> /V <sub>SS</sub>			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

**12 V SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $C_{DECOUPLING} = 0.1\ \mu\text{F}$ , unless otherwise noted.

**Table 3.**

Parameter	+25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0V to $V_{DD}$	V	$V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$ , see Figure 30
On Resistance, $R_{ON}$	22			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	24.5	31	37	$\Omega$ max	
	10			$\Omega$ typ	$V_S = 3.5\text{ V to }8.5\text{ V}$ , $I_S = -10\text{ mA}$
	11.2	14	16.5	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.05			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	0.5	0.6	0.7	$\Omega$ max	
	0.05			$\Omega$ typ	$V_S = 3.5\text{ V to }8.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.5	0.6	0.7	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			$\Omega$ typ	$V_S = 0\text{ V to }10\text{ V}$ , $I_S = -10\text{ mA}$
	14.5	19	23	$\Omega$ max	
	0.6			$\Omega$ typ	$V_S = 3.5\text{ V to }8.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.9	1.1	1.3	$\Omega$ max	
Threshold Voltage, $V_T$	0.7			V typ	See Figure 26
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ , see Figure 31
	$\pm 1.5$	$\pm 5.0$	$\pm 21.0$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ , see Figure 31
	$\pm 1.5$	$\pm 5.0$	$\pm 18.0$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.3$			nA typ	$V_S = V_D = 1\text{ V}/10\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 2.0$	$\pm 4.5$	nA max	
<b>FAULT</b>					
Source Leakage Current, $I_S$ With Overvoltage			$\pm 78$	$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 35
Power Supplies Grounded or Floating			$\pm 40$	$\mu\text{A}$ typ	$V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $I_{INx} = 0\text{ V}$ or floating, $V_S = \pm 55\text{ V}$ , see Figure 36
Drain Leakage Current, $I_D$ With Overvoltage	$\pm 2.0$			nA typ	$V_{DD} = 13.2\text{ V}$ , $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , see Figure 35
	$\pm 8.0$	$\pm 15.0$	$\pm 49.0$	nA max	
Power Supplies Grounded	$\pm 10$			nA typ	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $I_{INx} = 0\text{ V}$ , see Figure 36
	$\pm 30$	$\pm 50$	$\pm 100$	nA max	
Power Supplies Floating	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ typ	$V_{DD} = \text{floating}$ , $V_{SS} = \text{floating}$ , $GND = 0\text{ V}$ , $V_S = \pm 55\text{ V}$ , $I_{INx} = 0\text{ V}$ , see Figure 36
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2.0	V min	
Input Voltage Low, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.7			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$
			1.2	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	5.0			pF typ	
Output Voltage High, $V_{OH}$	2.0			V min	
Output Voltage Low, $V_{OL}$	0.8			V max	

Parameter	+25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	400			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	485	515	540	ns max	$V_S = 8 \text{ V}$ , see Figure 44
$t_{OFF}$	375			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	460	495	520	ns max	$V_S = 8 \text{ V}$ , see Figure 44
Overvoltage Response Time, $t_{RESPONSE}$	560		170	ns min	$V_{S1} = V_{S2} = 8 \text{ V}$ , see Figure 44
	660	700	720	ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 39
Overvoltage Recovery Time, $t_{RECOVERY}$	640			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 40
	800	865	960	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	$C_L = 10 \text{ pF}$ , see Figure 41
Interrupt Flag Recovery Time, $t_{DIGREC}$	60		85	$\mu\text{s}$ typ	$C_L = 10 \text{ pF}$ , see Figure 42
	600			ns typ	$C_L = 10 \text{ pF}$ , $R_{PULLUP} = 1 \text{ k}\Omega$ , see Figure 43
Charge Injection, $Q_{INJ}$	340			pC typ	$V_S = 6 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see Figure 45
Off Isolation	-65			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 33
Channel-to-Channel Crosstalk	-90			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 34
Total Harmonic Distortion Plus Noise, THD + N	0.007			% typ	$R_L = 10 \text{ k}\Omega$ , $V_S = 6 \text{ V p-p}$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , see Figure 38
-3 dB Bandwidth	270			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , see Figure 37
Insertion Loss	-0.74			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 37
$C_S$ (Off)	16			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (Off)	15			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)	25			pF typ	$V_S = 6 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$V_{DD} = 13.2 \text{ V}$ , $V_{SS} = 0 \text{ V}$ , digital inputs = 0 V, 5 V, or $V_{DD}$					
Normal Mode					
$I_{DD}$	0.9			mA typ	
	1.2		1.3	mA max	
$I_{GND}$	0.4			mA typ	
	0.55		0.6	mA max	
$I_{SS}$	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					$V_S = \pm 55 \text{ V}$
$I_{DD}$	1.2			mA typ	
	1.6		1.8	mA max	
$I_{GND}$	0.8			mA typ	
	1.0		1.1	mA max	
$I_{SS}$	0.5			mA typ	Digital inputs = 5 V
	1.0		1.8	mA max	$V_S = \pm 55 \text{ V}$ , $V_D = 0 \text{ V}$
$V_{DD}$			8	V min	$GND = 0 \text{ V}$
			44	V max	$GND = 0 \text{ V}$

<sup>1</sup> Guaranteed by design; not subject to production test.

**36 V SINGLE SUPPLY**

$V_{DD} = 36\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ ,  $C_{DECOUPLING} = 0.1\ \mu\text{F}$ , unless otherwise noted.

**Table 4.**

Parameter	+25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	$V_{DD} = 32.4\text{ V}$ , $V_{SS} = 0\text{ V}$ , see Figure 30
On Resistance, $R_{ON}$	22			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$
	24.5	31	37	$\Omega$ max	
	10			$\Omega$ typ	$V_S = 4.5\text{ V to }28\text{ V}$ , $I_S = -10\text{ mA}$
	11	14	16.5	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.05			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$
	0.5	0.6	0.7	$\Omega$ max	
	0.05			$\Omega$ typ	$V_S = 4.5\text{ V to }28\text{ V}$ , $I_S = -10\text{ mA}$
	0.35	0.5	0.5	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			$\Omega$ typ	$V_S = 0\text{ V to }30\text{ V}$ , $I_S = -10\text{ mA}$
	14.5	19	23	$\Omega$ max	
	0.1			$\Omega$ typ	$V_S = 4.5\text{ V to }28\text{ V}$ , $I_S = -10\text{ mA}$
	0.4	0.5	0.5	$\Omega$ max	
Threshold Voltage, $V_T$	0.7			V typ	See Figure 26
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = 0\text{ V}$
	$\pm 1.5$	$\pm 5.0$	$\pm 21.0$	nA max	$V_S = 1\text{ V}/30\text{ V}$ , $V_D = 30\text{ V}/1\text{ V}$ , see Figure 31
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S = 1\text{ V}/30\text{ V}$ , $V_D = 30\text{ V}/1\text{ V}$ , see Figure 31
	$\pm 1.5$	$\pm 5.0$	$\pm 18.0$	nA max	
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.3$			nA typ	$V_S = V_D = 1\text{ V}/30\text{ V}$ , see Figure 32
	$\pm 1.5$	$\pm 2.0$	$\pm 4.5$	nA max	
<b>FAULT</b>					
Source Leakage Current, $I_S$ With Overvoltage			$\pm 78$	$\mu\text{A}$ typ	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = +55\text{ V}$ , $-40\text{ V}$ , see Figure 35
Power Supplies Grounded or Floating			$\pm 40$	$\mu\text{A}$ typ	$V_{DD} = 0\text{ V}$ or floating, $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $I_{NX} = 0\text{ V}$ or floating, $V_S = +55\text{ V}$ , $-40\text{ V}$ , see Figure 36
Drain Leakage Current, $I_D$ With Overvoltage	$\pm 2.0$			nA typ	$V_{DD} = 39.6\text{ V}$ , $V_{SS} = 0\text{ V}$ or floating, $GND = 0\text{ V}$ , $V_S = +55\text{ V}$ , $-40\text{ V}$ , see Figure 35
	$\pm 8.0$	$\pm 15.0$	$\pm 49.0$	nA max	
Power Supplies Grounded	$\pm 10$			nA typ	$V_{DD} = 0\text{ V}$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , $V_S = +55\text{ V}$ , $-40\text{ V}$ , $I_{NX} = 0\text{ V}$ , see Figure 36
	$\pm 30$	$\pm 50$	$\pm 100$	nA max	
Power Supplies Floating	$\pm 10$	$\pm 10$	$\pm 10$	$\mu\text{A}$ typ	$V_{DD} = \text{floating}$ , $V_{SS} = \text{floating}$ , $GND = 0\text{ V}$ , $V_S = +55\text{ V}$ , $-40\text{ V}$ , $I_{NX} = 0\text{ V}$ , see Figure 36
<b>DIGITAL INPUTS</b>					
Input Voltage High, $V_{INH}$			2.0	V min	$V_{IN} = V_{GND}$ or $V_{DD}$
Input Voltage Low, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.7			$\mu\text{A}$ typ	
			1.2	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	5.0			pF typ	
Output Voltage High, $V_{OH}$	2.0			V min	
Output Voltage Low, $V_{OL}$	0.8			V max	

Parameter	+25°C	-40°C to +85°C	-55°C to +125°C	Unit	Test Conditions/Comments
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	400			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	490	520	545	ns max	$V_S = 18 \text{ V}$ , see Figure 44
$t_{OFF}$	375			ns typ	$R_L = 300 \Omega$ , $C_L = 35 \text{ pF}$
	460	485	510	ns max	$V_S = 18 \text{ V}$ , see Figure 44
Overvoltage Response Time, $t_{RESPONSE}$	250			ns typ	$V_{S1} = V_{S2} = 18 \text{ V}$ , see Figure 44
	350	360	375	ns max	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 39
Overvoltage Recovery Time, $t_{RECOVERY}$	1500			ns typ	$R_L = 1 \text{ k}\Omega$ , $C_L = 2 \text{ pF}$ , see Figure 40
	2000	2300	2700	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	85		115	ns typ	$C_L = 10 \text{ pF}$ , see Figure 41
Interrupt Flag Recovery Time, $t_{DIGREC}$	60		85	$\mu\text{s}$ typ	$C_L = 10 \text{ pF}$ , see Figure 42
Charge Injection, $Q_{INJ}$	600			ns typ	$C_L = 10 \text{ pF}$ , $R_{PULLUP} = 1 \text{ k}\Omega$ , see Figure 43
	610			pC typ	$V_S = 18 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ , see Figure 45
Off Isolation	-70			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 33
Channel-to-Channel Crosstalk	-90			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 34
Total Harmonic Distortion Plus Noise, THD + N	0.001			% typ	$R_L = 10 \text{ k}\Omega$ , $V_S = 18 \text{ V}$ p-p, $f = 20 \text{ Hz}$ to $20 \text{ kHz}$ , see Figure 38
-3 dB Bandwidth	270			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , see Figure 37
Insertion Loss	-0.75			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 1 \text{ MHz}$ , see Figure 37
$C_S$ (Off)	12			pF typ	$V_S = 18 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (Off)	11			pF typ	$V_S = 18 \text{ V}$ , $f = 1 \text{ MHz}$
$C_D$ (On), $C_S$ (On)	23			pF typ	$V_S = 18 \text{ V}$ , $f = 1 \text{ MHz}$
<b>POWER REQUIREMENTS</b>					
Normal Mode					$V_{DD} = 39.6 \text{ V}$ , $V_{SS} = 0 \text{ V}$ , digital inputs = 0 V, 5 V, or $V_{DD}$
$I_{DD}$	0.9			mA typ	
	1.2		1.3	mA max	
$I_{GND}$	0.4			mA typ	
	0.55		0.6	mA max	
$I_{SS}$	0.5			mA typ	
	0.65		0.7	mA max	
Fault Mode					$V_S = +55 \text{ V}$ , $-40 \text{ V}$
$I_{DD}$	1.2			mA typ	
	1.6		1.8	mA max	
$I_{GND}$	0.8			mA typ	
	1.0		1.1	mA max	
$I_{SS}$	0.5			mA typ	
	1.0		1.8	mA max	
$V_{DD}$			8	V min	GND = 0 V
			44	V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

**CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx**

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
16-LEAD TSSOP $\theta_{JA} = 112.6^{\circ}\text{C}/\text{W}$	83	59	39	mA max	$V_S = V_{SS} + 4.5\text{ V}$ to $V_{DD} - 4.5\text{ V}$
	64	48	29	mA max	$V_S = V_{SS}$ to $V_{DD}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 6.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	48 V
$V_{DD}$ to GND	-0.3 V to +48 V
$V_{SS}$ to GND	-48 V to +0.3 V
Sx Pins to GND	-55 V to +55 V
Sx to $V_{DD}$ or $V_{SS}$	80 V
$V_S$ to $V_D$	80 V
Dx Pins <sup>1</sup>	$V_{SS} - 0.7\text{ V}$ to $V_{DD} + 0.7\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs	GND - 0.3 V to +48 V
Peak Current, Sx or Dx Pins	288 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx Pins	Data <sup>2</sup> + 15%
Digital Output	GND - 0.3 V to 6 V or 30 mA, whichever occurs first
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, $\theta_{JA}$	
16-Lead TSSOP, $\theta_{JA}$ Thermal Impedance (4-Layer Board)	112.6°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
ESD (HBM: ANSI/ESD STM5.1-2007)	
Input/Output Port to Supplies	5.5 kV
Input/Output Port to Input/Output Port	5.5 kV
All Other Pins	5.5 kV

<sup>1</sup> Overvoltages at the Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

<sup>2</sup> See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

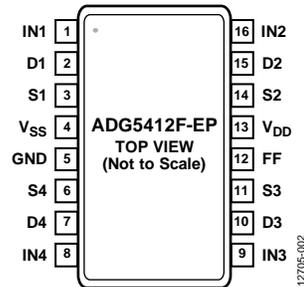


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	Logic Control Input.
2	D1	Drain Terminal. This pin can be an input or an output.
3	S1	Overvoltage Protected Source Terminal. This pin can be an input or an output.
4	V <sub>SS</sub>	Most Negative Power Supply Potential.
5	GND	Ground (0 V) Reference.
6	S4	Overvoltage Protected Source Terminal. This pin can be an input or an output.
7	D4	Drain Terminal. This pin can be an input or an output.
8	IN4	Logic Control Input.
9	IN3	Logic Control Input.
10	D3	Drain Terminal. This pin can be an input or an output.
11	S3	Overvoltage Protected Source Terminal. This pin can be an input or an output.
12	FF	Fault Flag Digital Output. This pin has a high output when the device is in normal operation or a low output when a fault condition occurs on any of the Sx inputs.
13	V <sub>DD</sub>	Most Positive Power Supply Potential.
14	S2	Overvoltage Protected Source Terminal. This pin can be an input or an output.
15	D2	Drain Terminal. This pin can be an input or an output.
16	IN2	Logic Control Input.

Table 8. ADG5412F-EP Truth Table

INx	Switch Condition (S1 to S4)
1	On
0	Off

TYPICAL PERFORMANCE CHARACTERISTICS

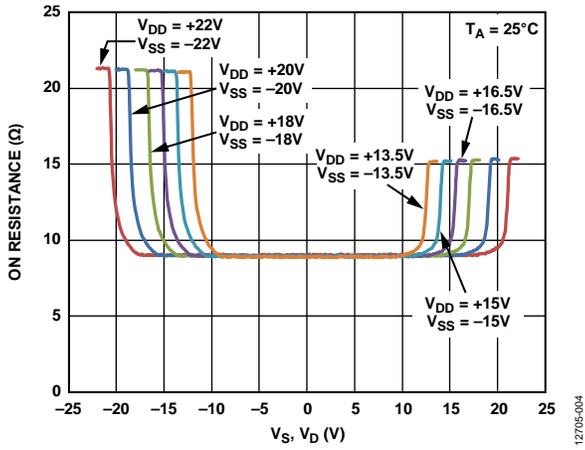


Figure 3.  $R_{ON}$  as a Function of  $V_S, V_D$  (Dual Supply)

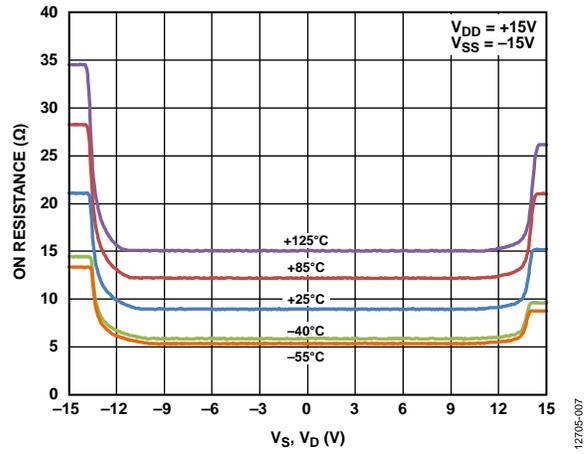


Figure 6.  $R_{ON}$  as a Function of  $V_S, V_D$  for Different Temperatures,  $\pm 15$  V Dual Supply

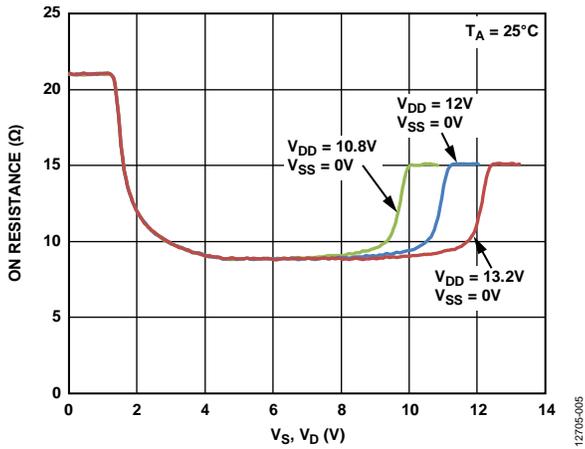


Figure 4.  $R_{ON}$  as a Function of  $V_S, V_D$  (12 V Single Supply)

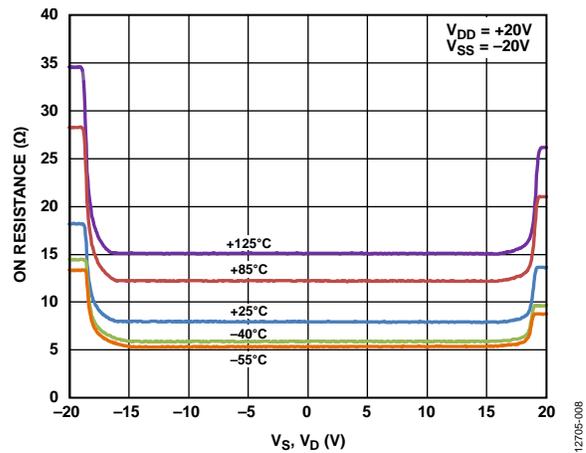


Figure 7.  $R_{ON}$  as a Function of  $V_S, V_D$  for Different Temperatures,  $\pm 20$  V Dual Supply

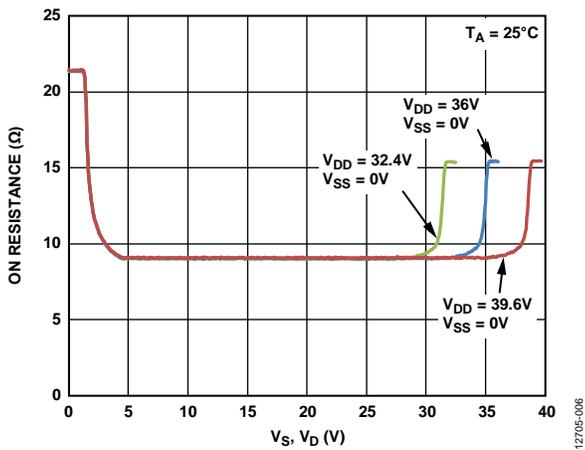


Figure 5.  $R_{ON}$  as a Function of  $V_S, V_D$  (36 V Single Supply)

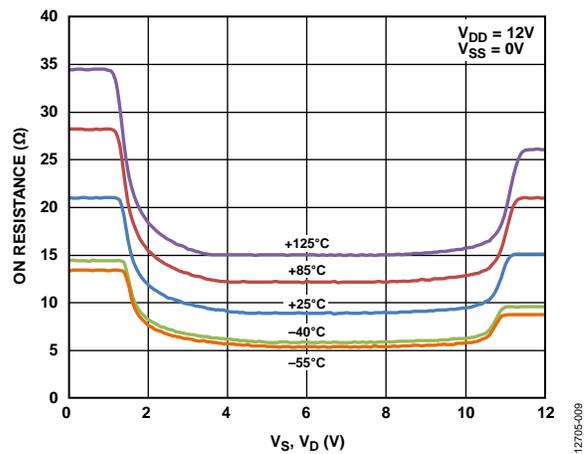


Figure 8.  $R_{ON}$  as a Function of  $V_S, V_D$  for Different Temperatures, 12 V Single Supply

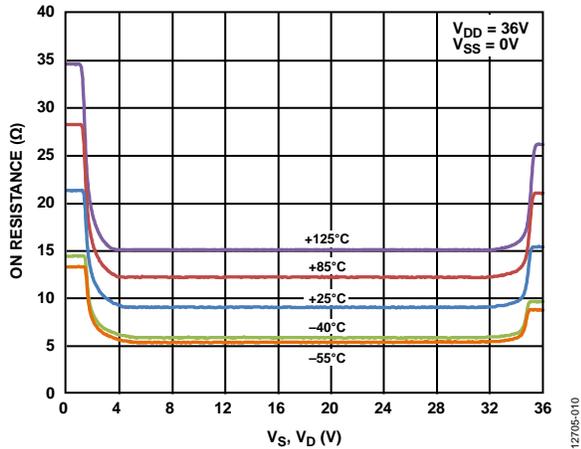


Figure 9.  $R_{ON}$  as a Function of  $V_S$ ,  $V_D$  for Different Temperatures, 36 V Single Supply

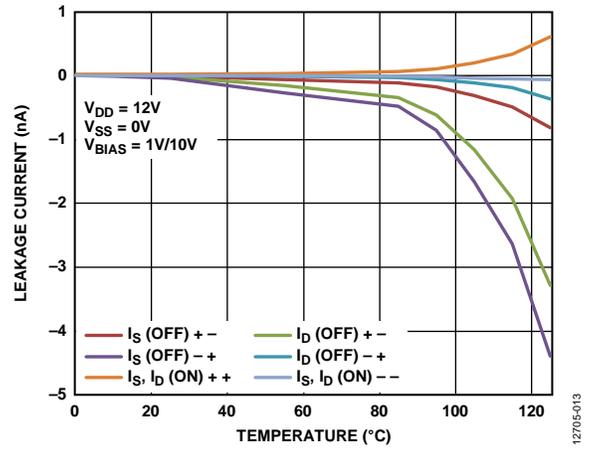


Figure 12. Leakage Current vs. Temperature, 12 V Single Supply

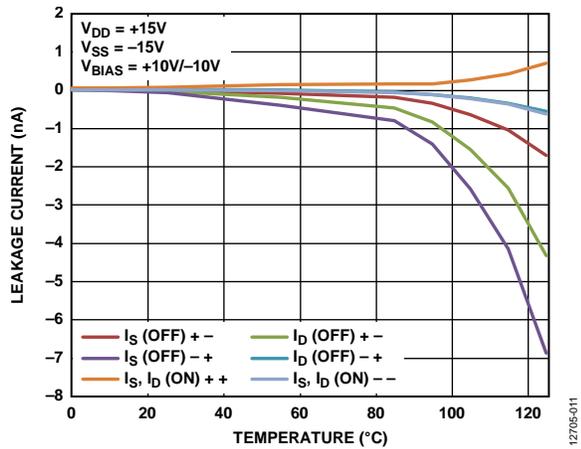


Figure 10. Leakage Current vs. Temperature,  $\pm 15$  V Dual Supply

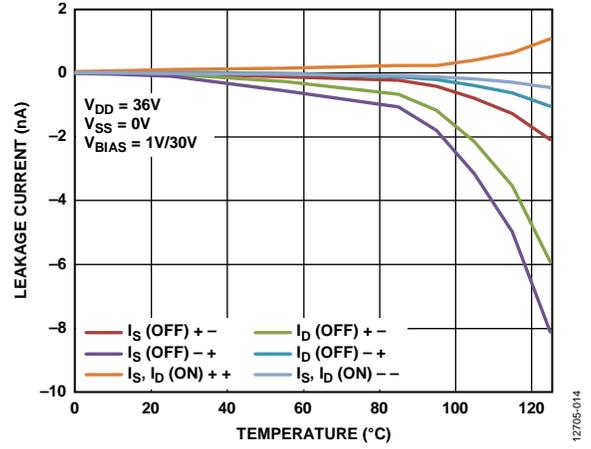


Figure 13. Leakage Current vs. Temperature, 36 V Single Supply

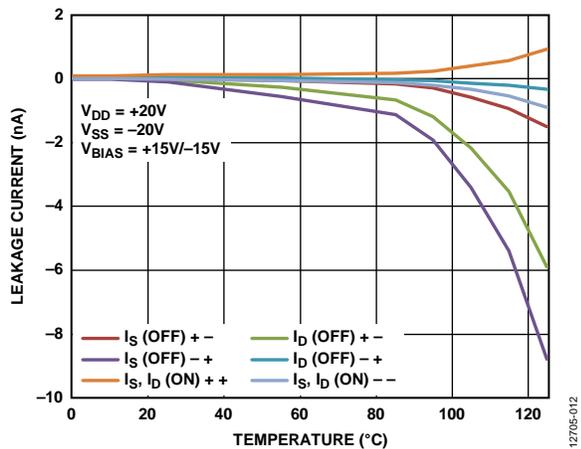


Figure 11. Leakage Current vs. Temperature,  $\pm 20$  V Dual Supply

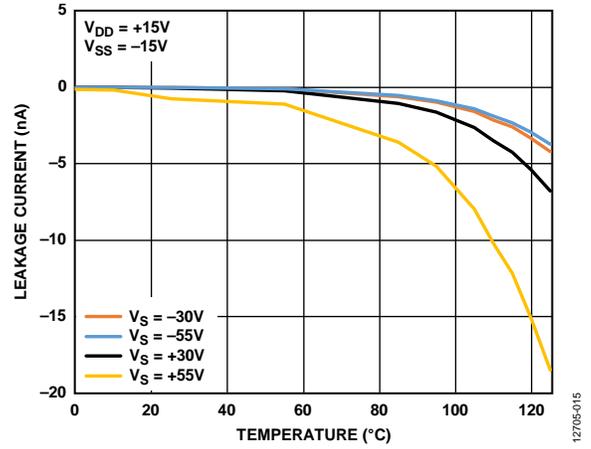


Figure 14. Overvoltage Leakage Current vs. Temperature,  $\pm 15$  V Dual Supply

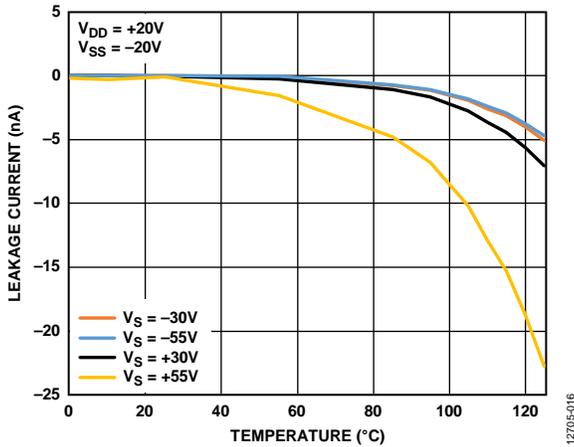


Figure 15. Overvoltage Leakage Current vs. Temperature, ±20V Dual Supply

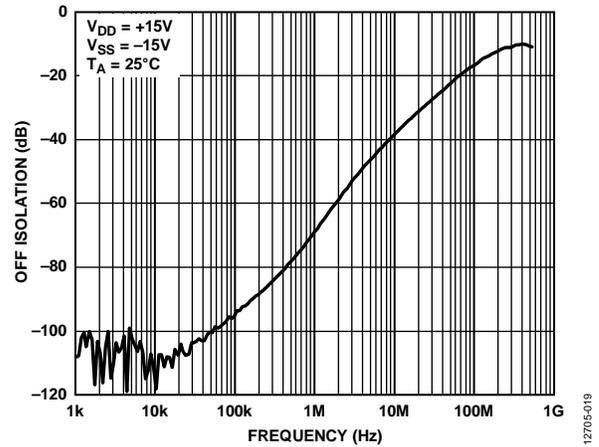


Figure 18. Off Isolation vs. Frequency, ±15V Dual Supply

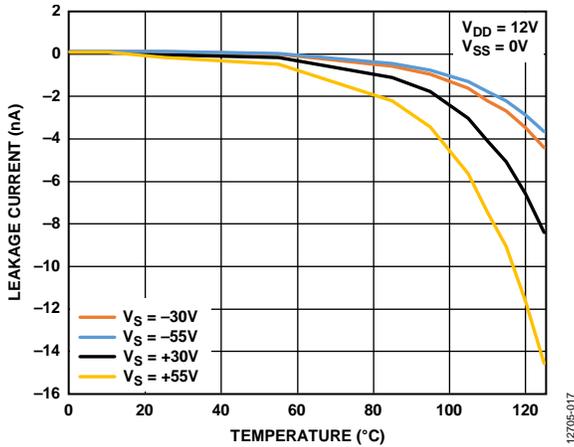


Figure 16. Overvoltage Leakage Current vs. Temperature, 12V Single Supply

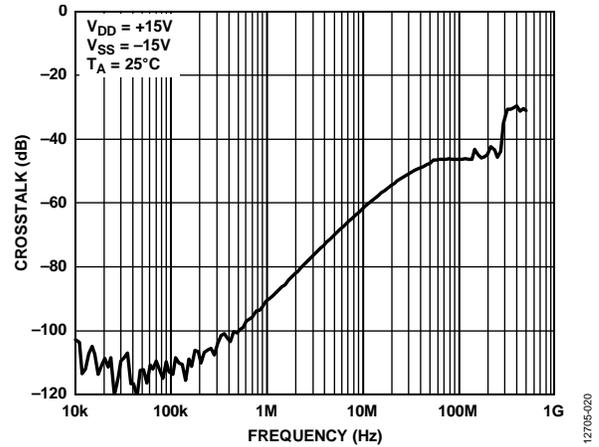


Figure 19. Crosstalk vs. Frequency, ±15V Dual Supply

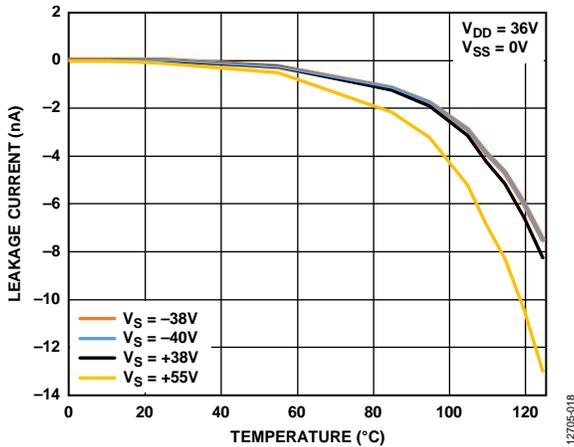


Figure 17. Overvoltage Leakage Current vs. Temperature, 36V Single Supply

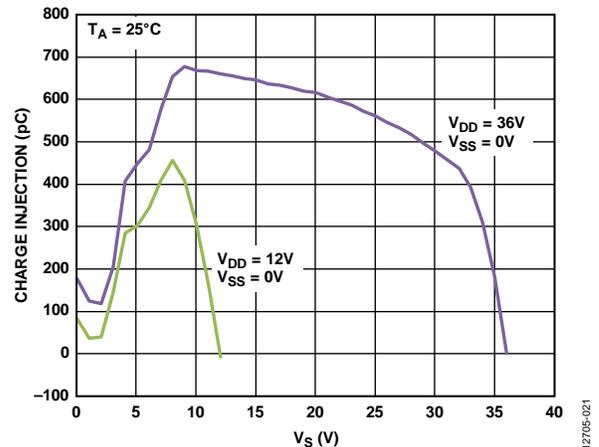


Figure 20. Charge Injection vs. Source Voltage (VS), Single Supply

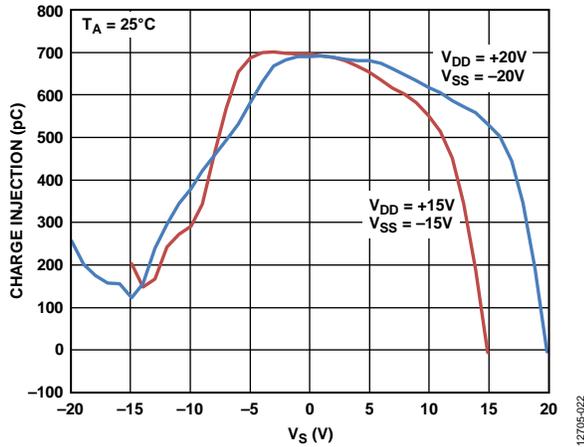


Figure 21. Charge Injection vs. Source Voltage ( $V_S$ ), Dual Supply

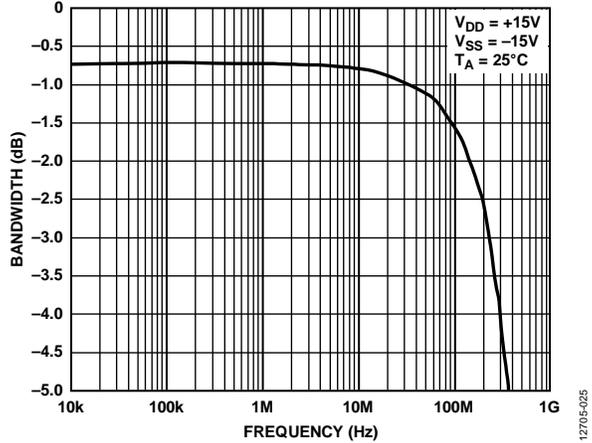


Figure 24. Bandwidth vs. Frequency,  $\pm 15$  V Dual Supply

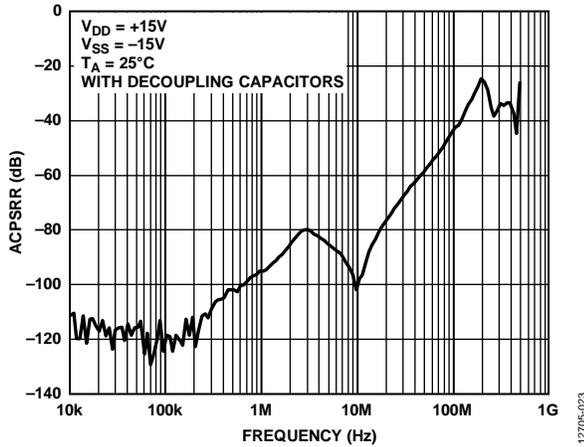


Figure 22. ACPSRR vs. Frequency,  $\pm 15$  V Dual Supply

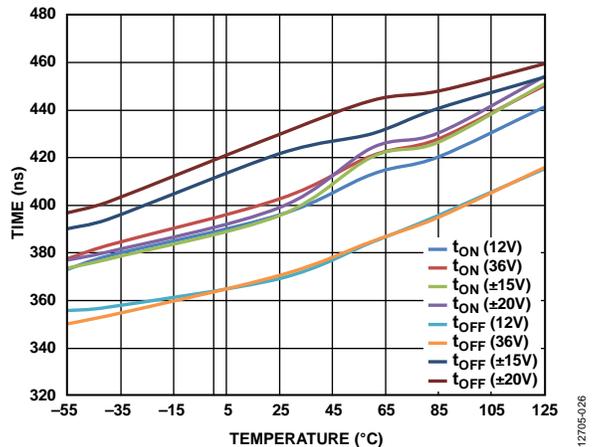


Figure 25.  $t_{ON}$ ,  $t_{OFF}$  Times vs. Temperature

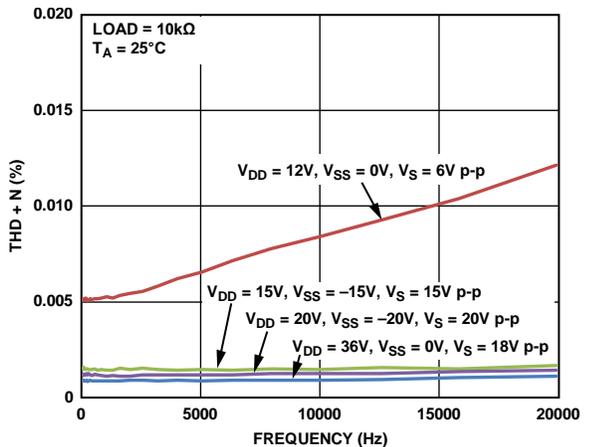


Figure 23. THD + N vs. Frequency

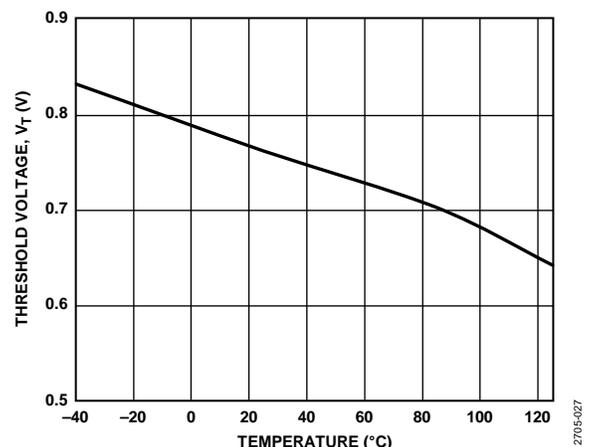


Figure 26. Threshold Voltage ( $V_T$ ) vs. Temperature

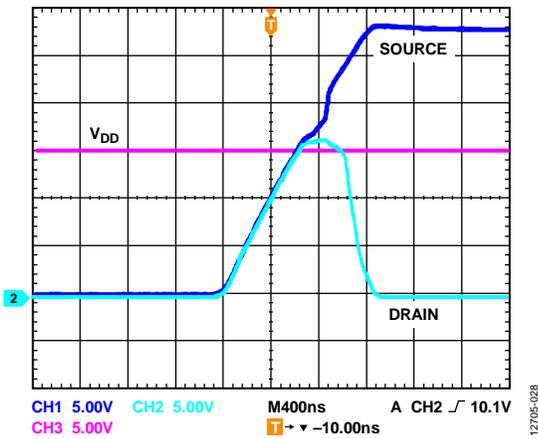


Figure 27. Drain Output Response to Positive Overvoltage

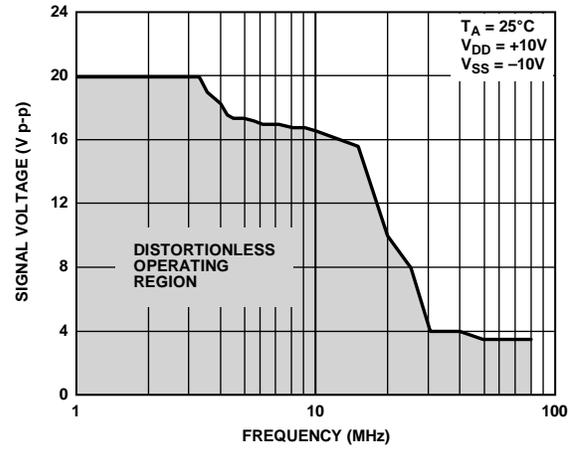


Figure 29. Large Signal Voltage Tracking vs. Frequency

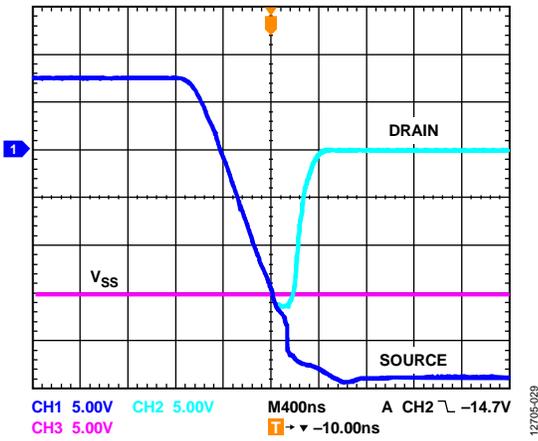


Figure 28. Drain Output Response to Negative Overvoltage

TEST CIRCUITS

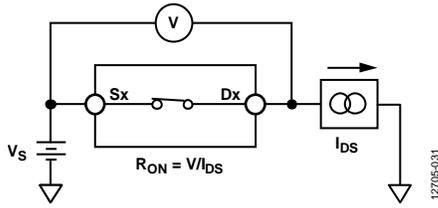


Figure 30. On Resistance

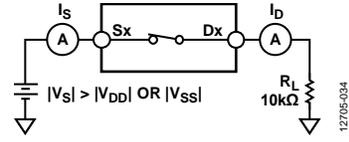


Figure 35. Switch Overvoltage Leakage

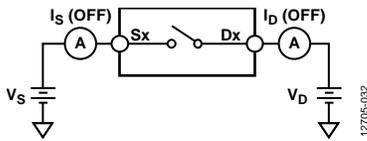


Figure 31. Off Leakage

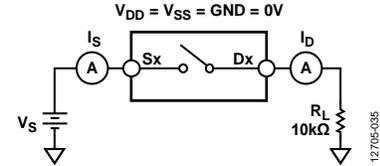


Figure 36. Switch Unpowered Leakage

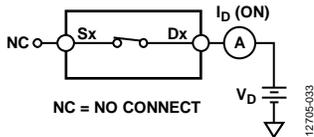


Figure 32. On Leakage

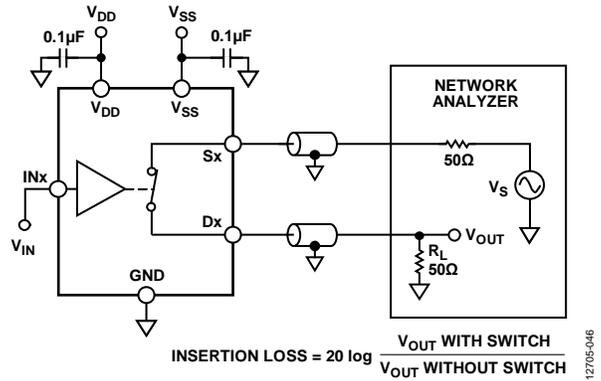


Figure 37. Bandwidth

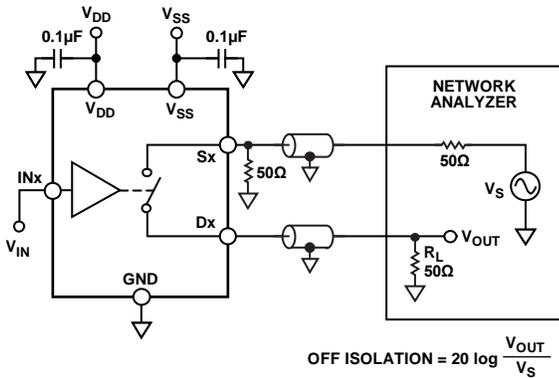


Figure 33. Off Isolation

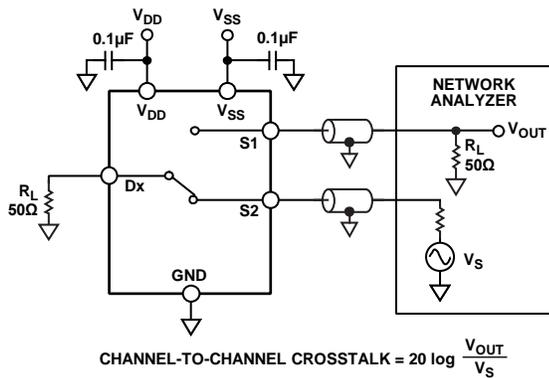


Figure 34. Channel-to-Channel Crosstalk

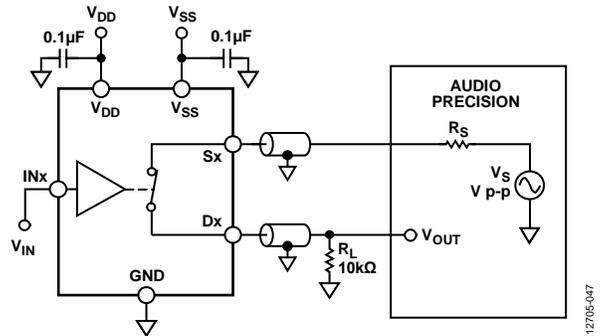
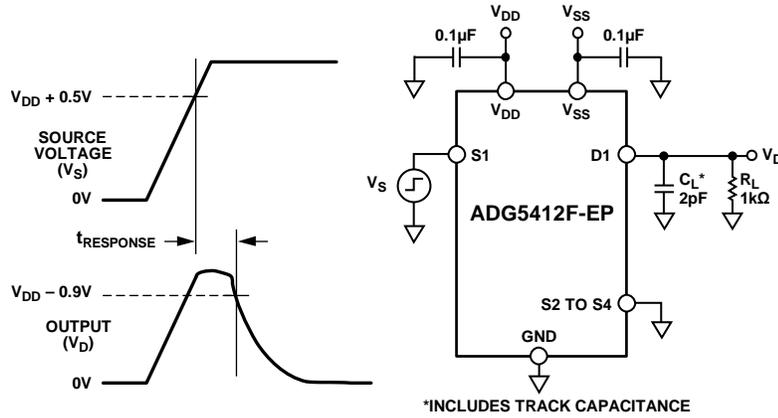
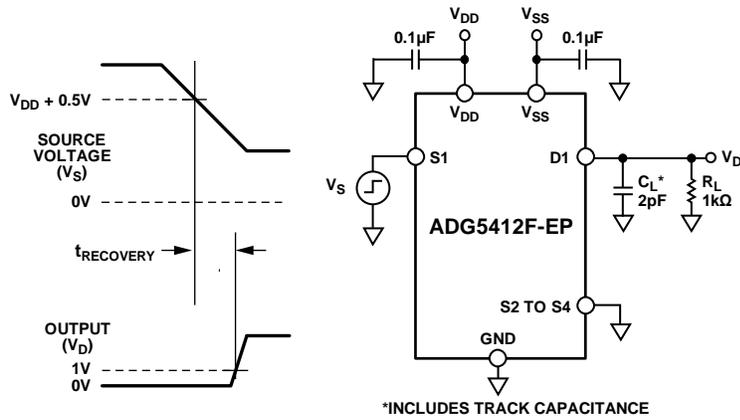


Figure 38. THD + N



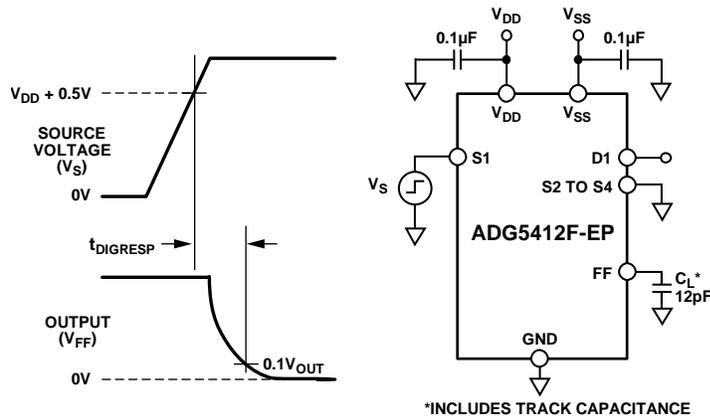
12705-036

Figure 39. Overvoltage Response Time,  $t_{RESPONSE}$



12705-037

Figure 40. Overvoltage Recovery Time,  $t_{RECOVERY}$



12705-038

Figure 41. Interrupt Flag Response Time,  $t_{DIGRESP}$

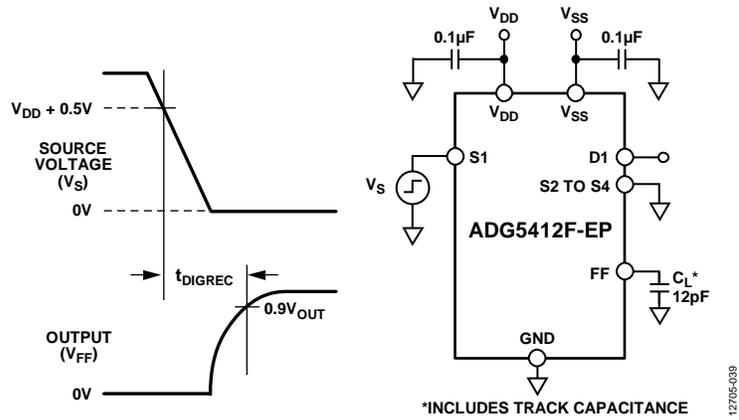


Figure 42. Interrupt Flag Recovery Time,  $t_{DIGREC}$

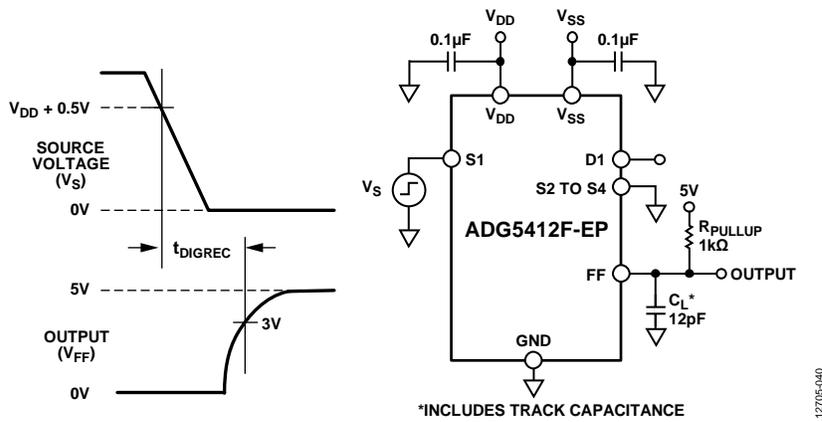


Figure 43. Interrupt Flag Recovery Time,  $t_{DIGREC}$ , with a 1 k $\Omega$  Pull-Up Resistor

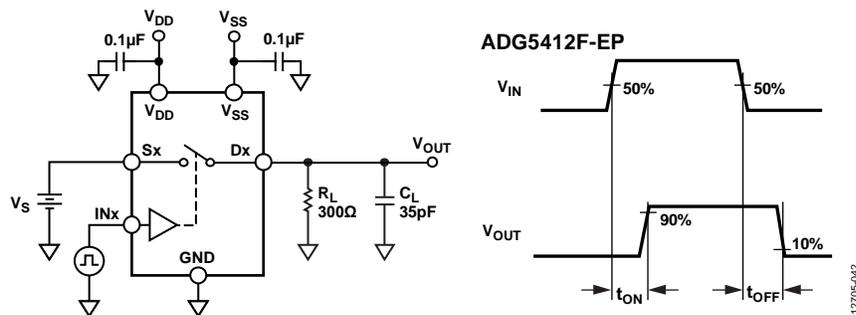


Figure 44. Switching Times,  $t_{ON}$  and  $t_{OFF}$

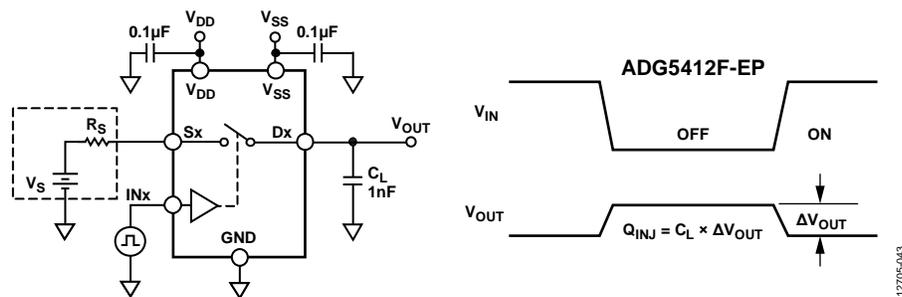
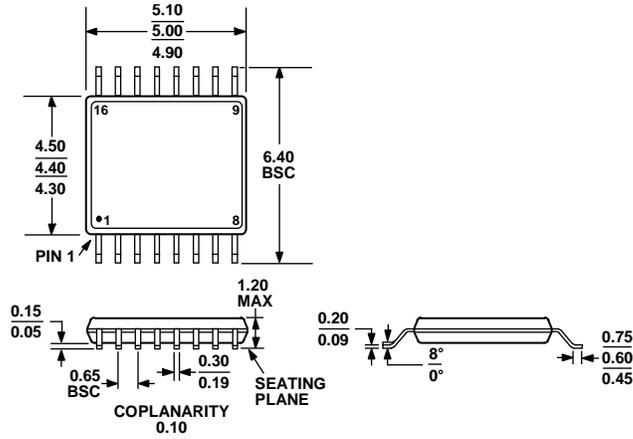


Figure 45. Charge Injection,  $Q_{INJ}$

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 46. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADG5412FTRUZ-EP	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5412FTRUZ-EP-R7	-55°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16

<sup>1</sup> Z = RoHS Compliant Part.