

Features

- Single line bidirectional protection
- Very low capacitance (1.2 pF max)
- Lead-free package
- Very low capacitance, line to ground, for optimized data integrity
- Low PCB space consumption: 0.18 mm² max
- No insertion loss in AM and FM band
- High reliability offered by monolithic integration

Complies with the following standards

- IEC 61000-4-2:
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883G- Method 3015-7: class 3B

Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Portable audio systems
- Communication systems
- Cellular phone handsets and accessories
- Audio and video equipment

Description

The ESDARF01-1BF4 is a monolithic application specific device dedicated to ESD protection of the AM and FM antenna in cell phones and portable equipment.

The device is ideal for applications where both reduced printed circuit board space and power absorption capability are required.

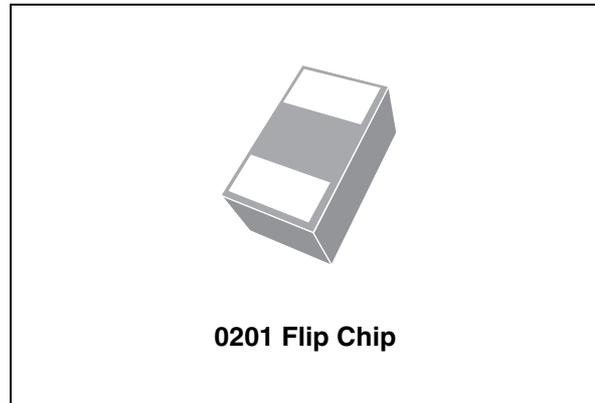
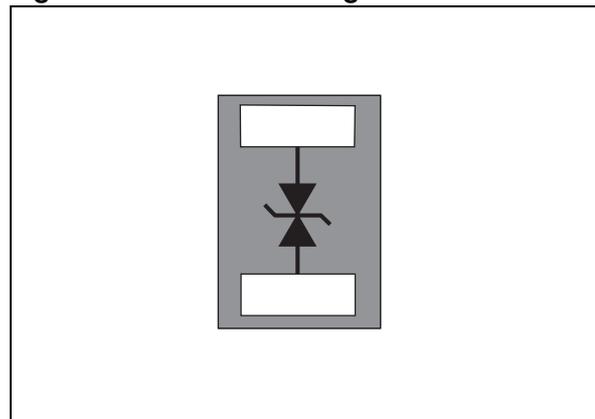


Figure 1. Functional diagram



1 Characteristics

Table 1. Absolute maximum ratings

Symbol	Parameter		Value	Unit
$V_{PP}^{(1)}$	Peak pulse voltage	IEC 61000-4-2 contact discharge	10	kV
		IEC 61000-4-2 air discharge	15	
T_j	Maximum operating junction temperature		125	°C
T_{stg}	Storage temperature range		- 55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s at 5 mm for case		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

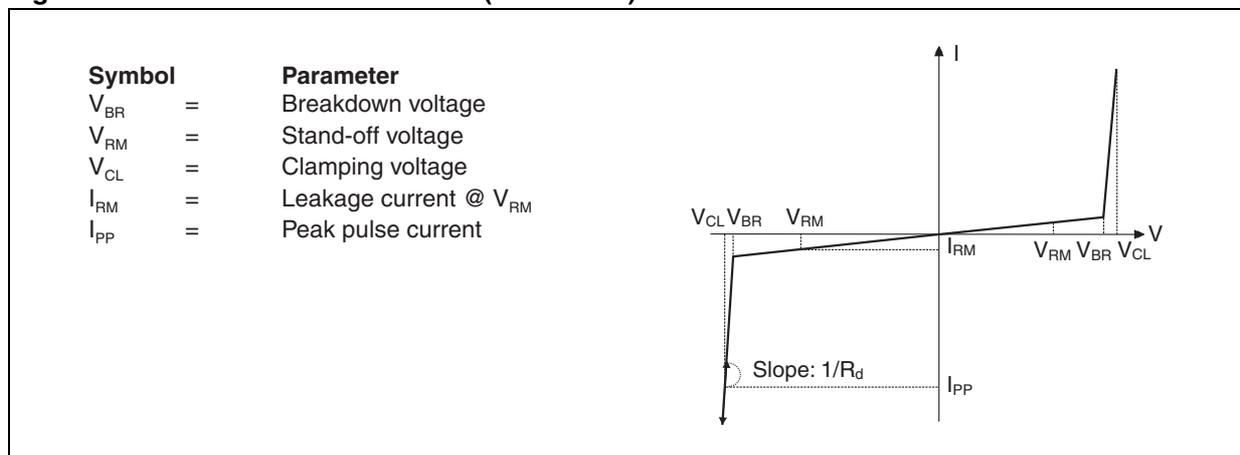


Table 2. Electrical characteristics (values, $T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{BR}	Breakdown voltage	$I_R = 1\text{ mA}$	0.6	0.8	1.0	V
I_{RM}	Leakage Current	$V_{RM} = 100\text{ mV}$			50	nA
$C_{i/o-GND}$	Capacitance between I/O and GND	$V_R = 0\text{ V}$, $F = 1\text{ MHz}$, any I/O pin to GND			1.2	pF

Figure 3. Dynamical resistance measurements

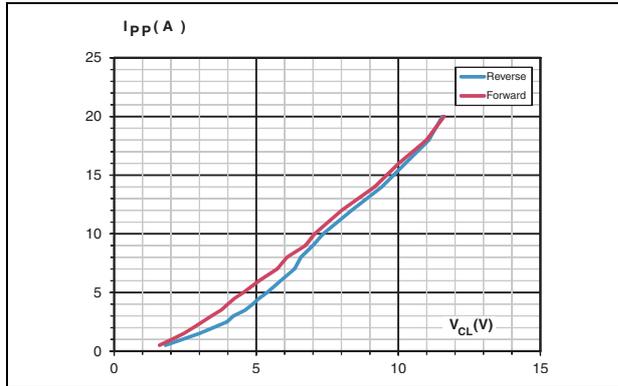


Figure 4. S21 attenuation measurements (50 Ω / 50 Ω)

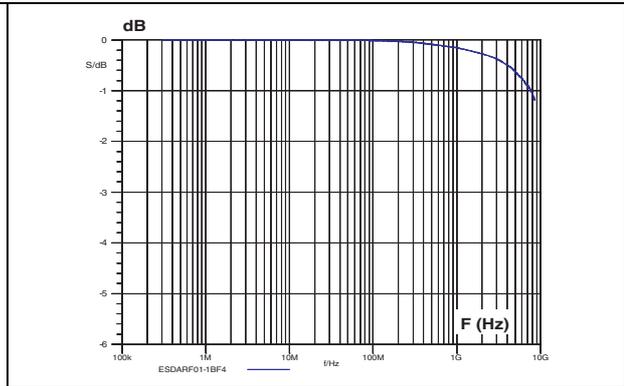


Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

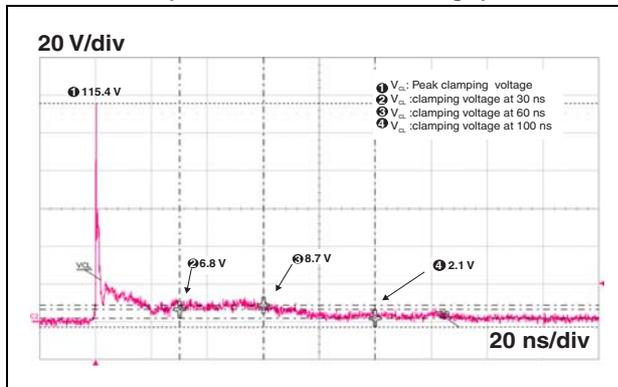


Figure 6. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

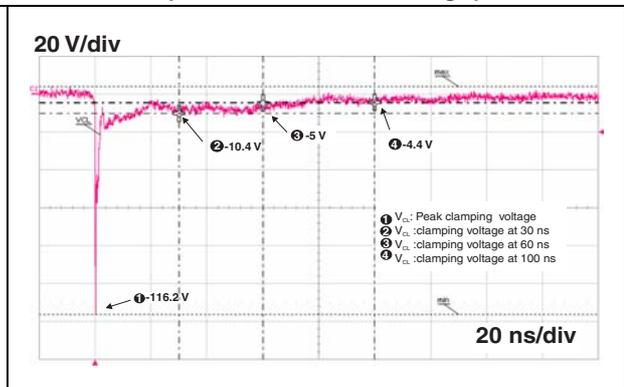


Figure 7. Junction capacitance versus reverse applied voltage (typical values)

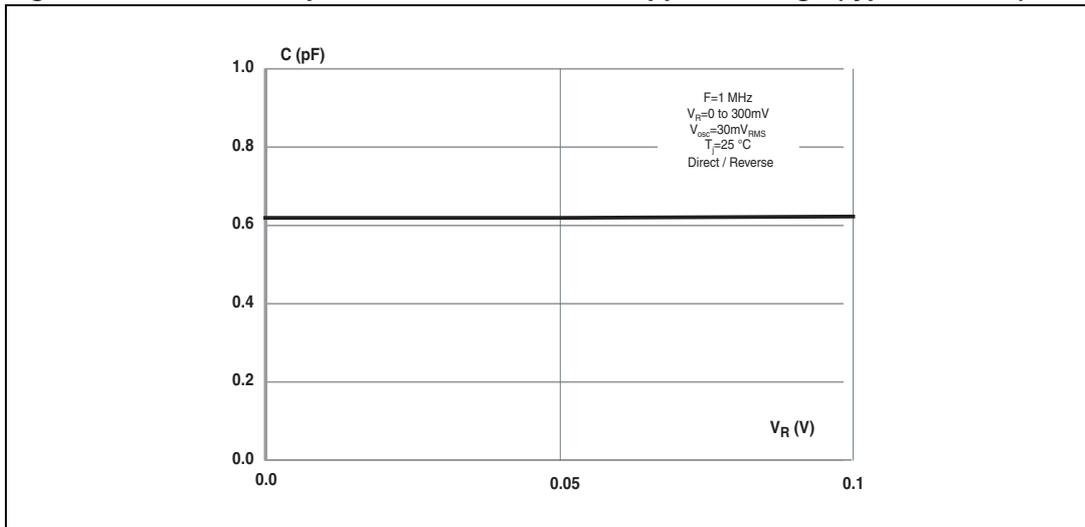
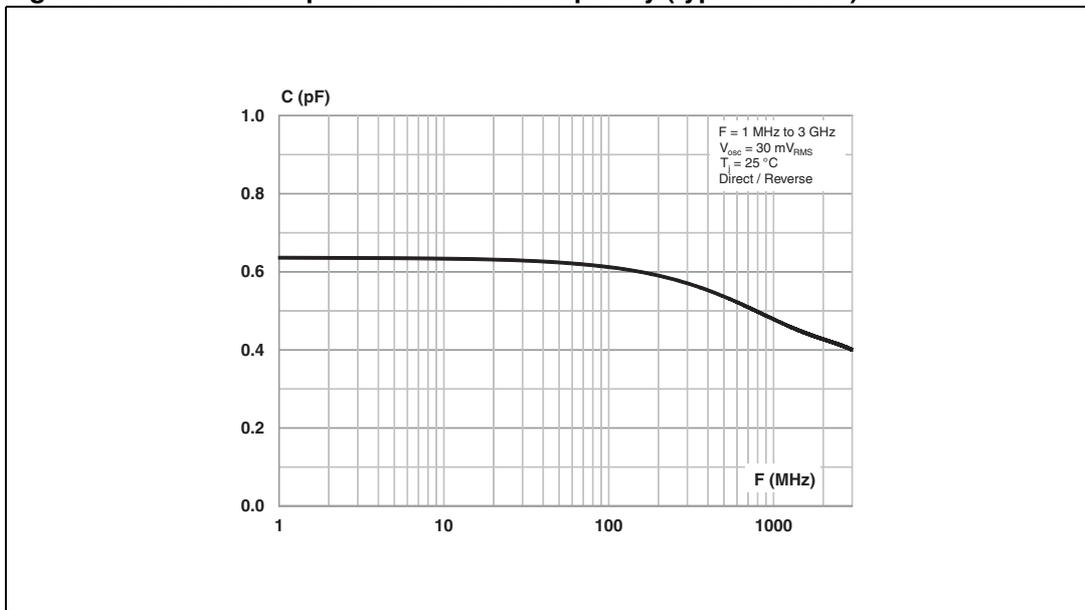
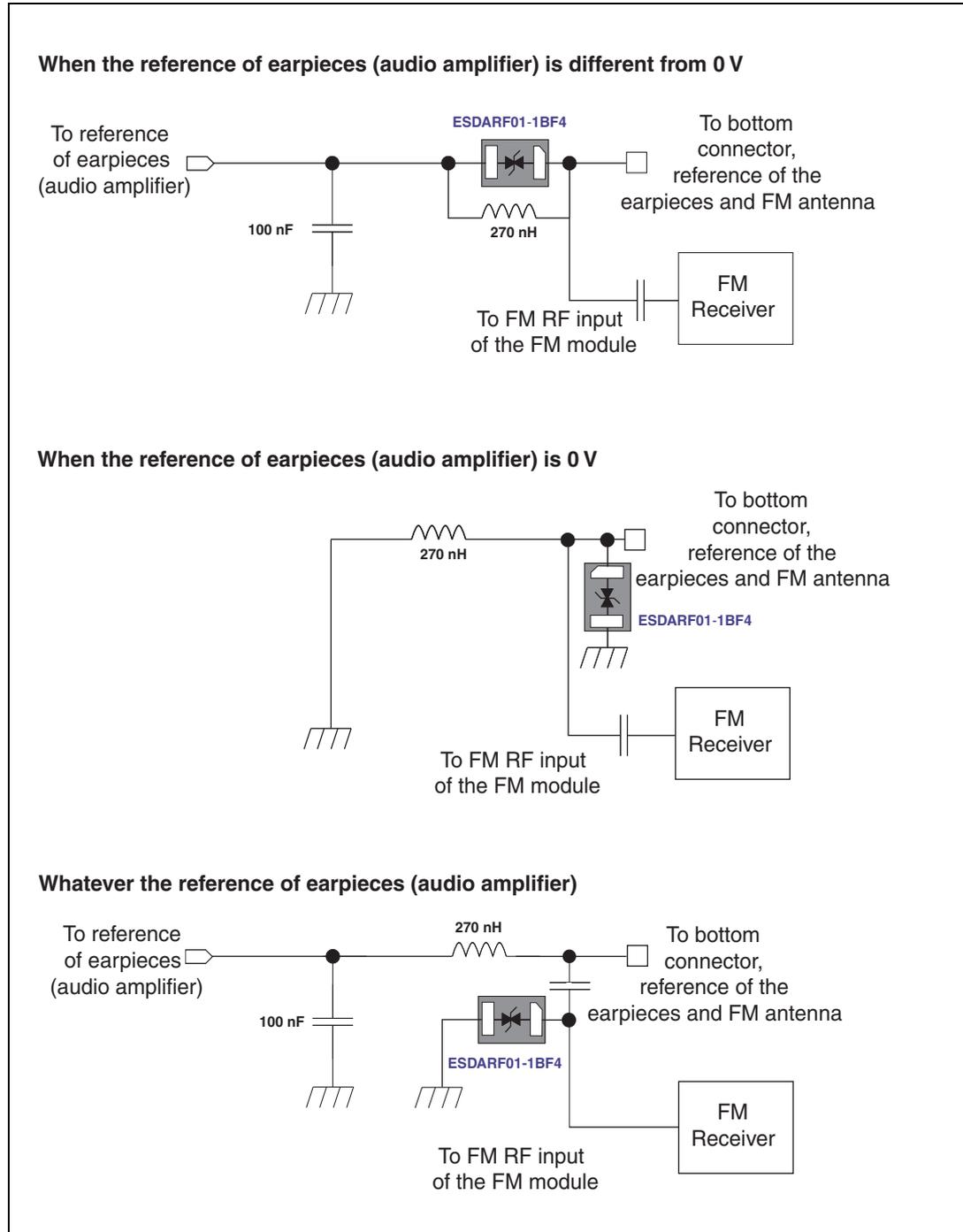


Figure 8. Junction capacitance versus frequency (typical values)



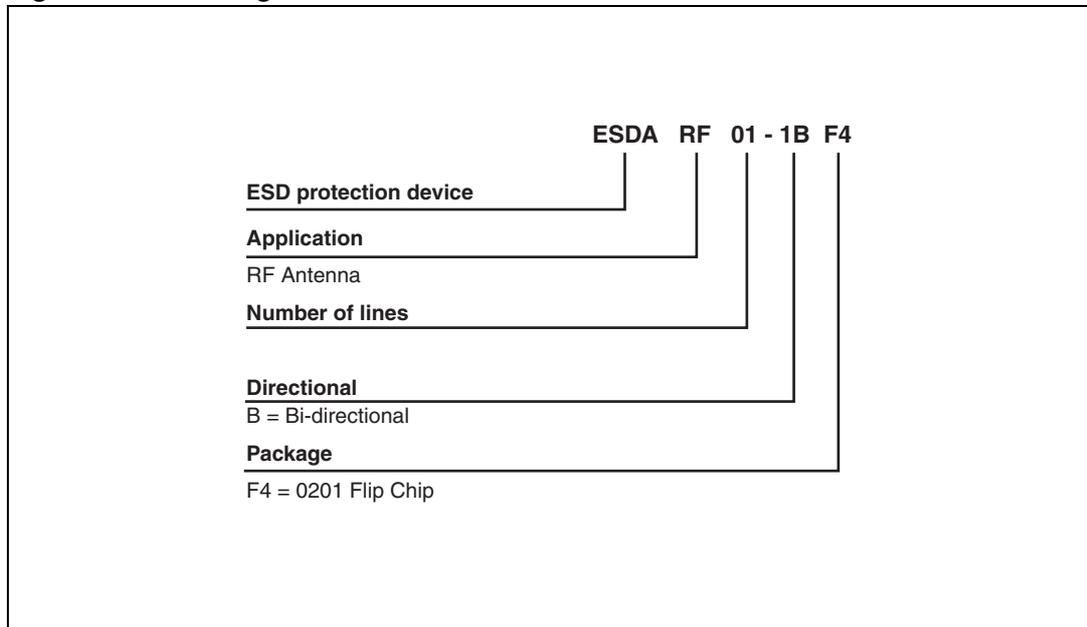
2 Application schematics

Figure 9. Application schematics



3 Ordering information scheme

Figure 10. Ordering information scheme



4 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 11. 0201 Flip Chip dimension definitions

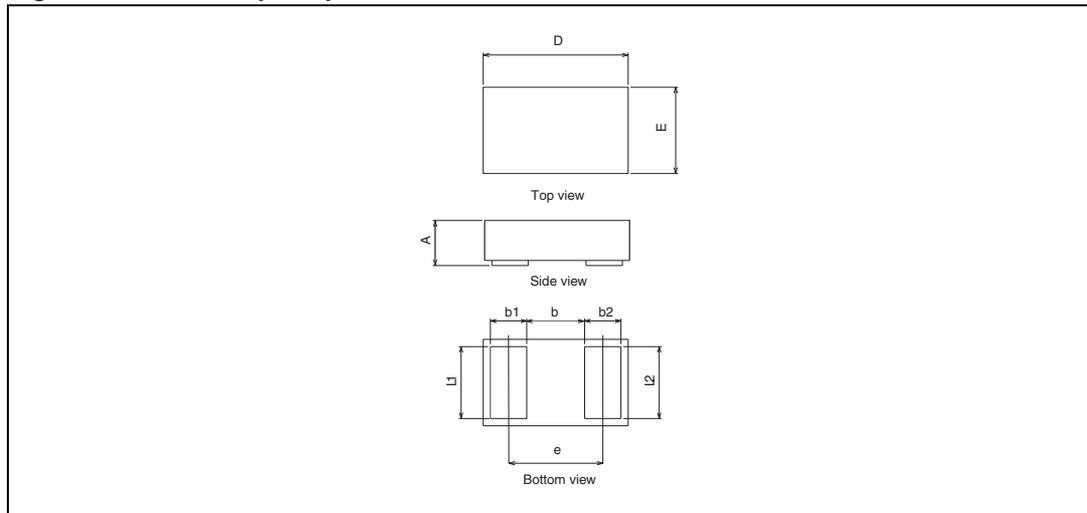


Table 3. 0201 Flip Chip dimension values

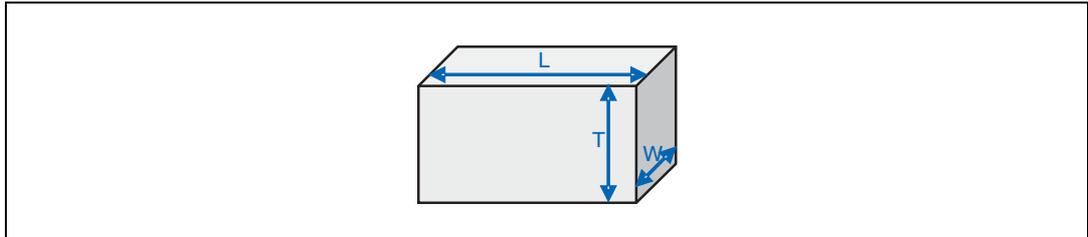
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.28	0.30	0.32	0.0110	0.0118	0.0126
b	0.19	0.21	0.23	0.0075	0.0082	0.0091
b1	0.125	0.14	0.155	0.0049	0.0055	0.0061
b2	0.125	0.14	0.155	0.0049	0.0055	0.0061
D	0.57	0.60	0.63	0.0224	0.0236	0.0257
e	0.33	0.35	0.37	0.0130	0.0138	0.0146
E	0.27	0.30	0.33	0.0106	0.0118	0.0130
L1	0.175	0.19	0.205	0.0069	0.0075	0.0081
L2	0.175	0.19	0.205	0.0069	0.0075	0.0081

5 Recommendation on PCB assembly

5.1 Stencil opening design

1. General recommendation on stencil opening design
 - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

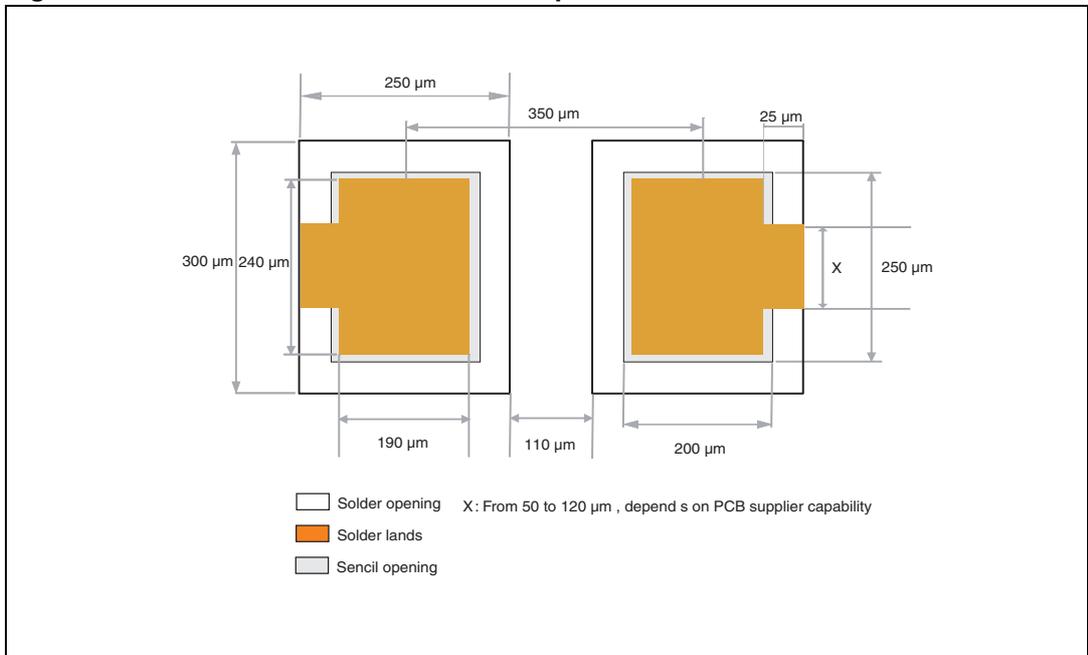
Figure 14. Stencil opening dimensions



- b) General design rule
 - Stencil thickness (T) = 75 ~ 125 μm
 - Aspect Ratio = $\frac{W}{T} \geq 1.5$
 - Aspect Area = $\frac{L \times W}{2T(L + W)} \geq 0.66$

2. Reference design
 - a) Stencil opening thickness: 100 μm
 - b) Stencil opening for leads: Opening to footprint ratio is 60% to 75%.

Figure 15. Recommended stencil window position



5.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 μm .

5.3 Placement

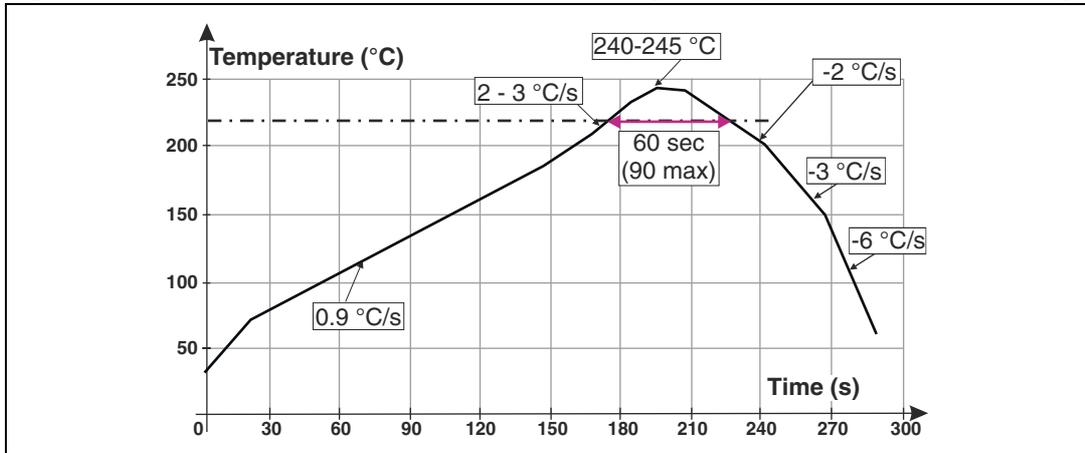
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.5 Reflow profile

Figure 16. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDARF01-1BF4	R	0201 Flip Chip	0.116 mg	15000	Tape and reel

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
16-Jan-2013	1	First issue

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