5V/12V Synchronous Buck PWM DC-DC Controller

General Description

The RT8106/A is a DC/DC synchronous buck PWM controller with embedded driver support up to 12V+12V boot-strapped voltage for high efficiency power driving. The part integrates full functions of voltage regulation, power monitoring and protection into a single small footprint WDFN-10L 3x3 (Exposed Pad) package.

The RT8106/A adopts a high-gain voltage mode PWM control for simple application design. An internal 0.8V reference allows the output voltage to be precisely regulated for low voltage requirement. Based on all RT8106/A features, the part provides an optimum compromise between efficiency, total B.O.M. count, and cost.

Ordering Information

RT8106/A □□

- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  P : Pb Free
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)
- 600kHz
- 300kHz

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

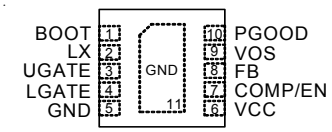
- **Single 5 to 12V Bias Supply**
- **Drive All Low Cost N-MOSFETs**
- **Support High Current Application up to 30A**
- **High-Gain Voltage Mode PWM Control**
- **300kHz/600kHz Fixed Frequency Oscillator**
- **Fast Transient Response :**
  - **High-Speed EA Amplifier**
  - **0 to 85% Duty Ratio**
  - **External Compensation in The Control Loop**
- **Internal Soft-Start**
- **Adaptive Non-Overlapping Gate Driver**
- **Over Current Fault Monitor on low side MOSFET**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Graphic Card
- Motherboard, Desktop Servers
- IA and Telecom Equipment
- General High Power DC/DC Regulator

Pin Configurations

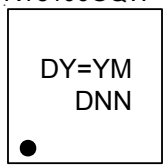
(TOP VIEW)



WDFN-10L 3x3

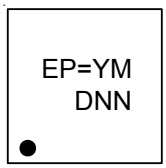
Marking Information

RT8106GQW



DY= : Product Code
YMDNN : Date Code

RT8106AGQW



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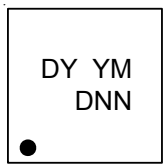
RT8106ZQW



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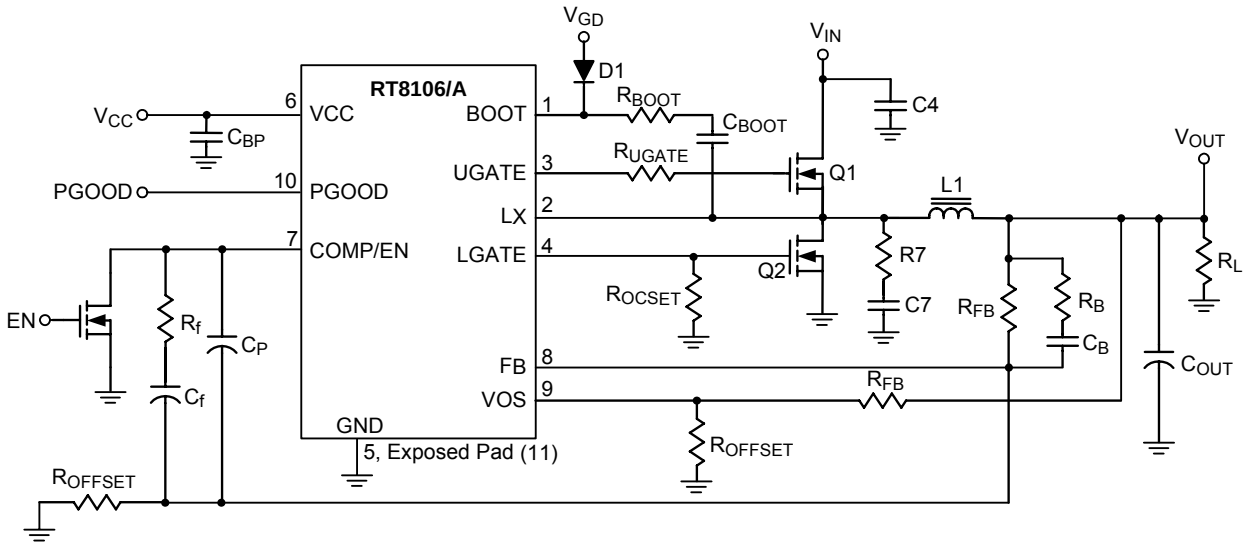
RT8106AZQW

EP : Product Code
YMDNN : Date Code

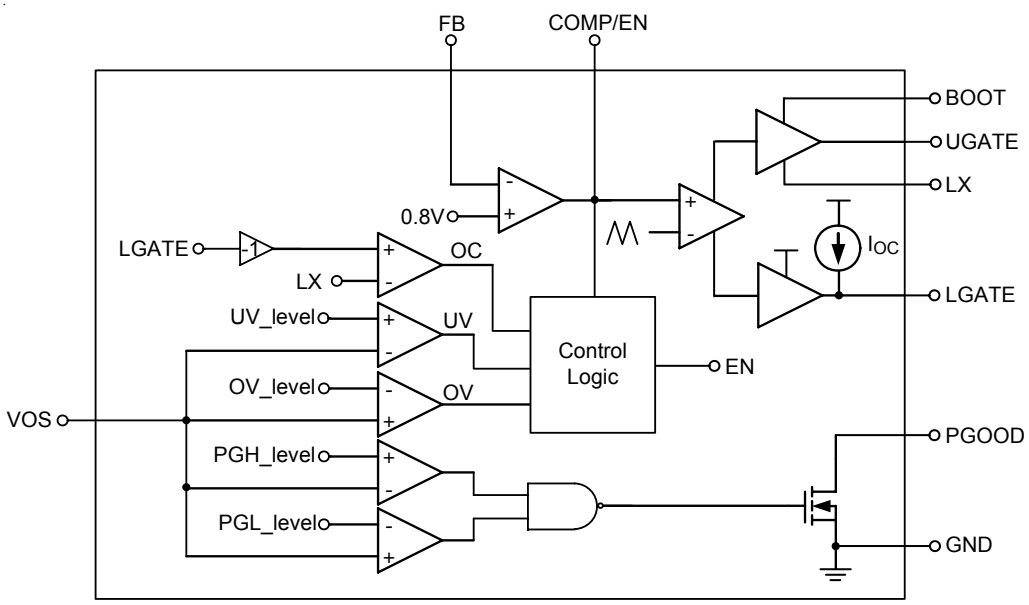
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	This pin is boot-strapped by external capacitor and is applied for the embedded High Side gate driver power.
2	LX	Phase node of PWM.
3	UGATE	High Side gate drive.
4	LGATE	Low Side gate drive. It also acts as OC setup pin by adjusting a resistor connecting to GND.
5, 11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	VCC	VCC is generally applied for bias power for IC logics and gate driver control. To connect a 1μF bypass capacitor to GND is recommended.
7	COMP/EN	Compensation pin of PWM and Output of the PWM error amplifier. Connect compensation network between this pin and FB. This pin is also applied as Enable pin.
8	FB	PWM Feedback. The output feedback of PWM. The pin is applied for voltage regulation.
9	VOS	The pin is scaled to be 0.8v and provides under voltage protection, over voltage protection and PGOOD function.
10	PGOOD	This pin is an open drain driver and Indicates PWM output regulated in +/-10%.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 15V
- BOOT to LX ---------- 15V
- Input, Output or I/O Voltage ---------- (GND–0.3V) to 7V
- LX to GND
  - DC ---------- –5V to 18V
  - < 200ns ---------- –10V to 30V
- BOOT to GND
  - DC ---------- –0.3V to 30V
  - < 200ns ---------- –0.3V to 42V
- UGATE ---------- (V_{LX} – 0.3V) to (V_{BOOT} + 0.3V)
  - < 200ns ---------- (V_{LX} – 5V) to (V_{BOOT} + 5V)
- LGATE ---------- (GND – 0.3V) to(V_{CC} + 0.3V)
  - < 200ns ---------- (GND – 5V) to (V_{CC} + 5V)
- Power Dissipation, P_D @ T_A = 25°C (Note 2)
  - WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance
  - WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 12V ± 10%, 5V ± 5%
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
Supply Input Voltage	V_{CC}		4.75	12	13.2	V
Nominal Supply Current	I_{CC}	No Load for UGATE/ LGATE	--	4	--	mA
VCC POR Threshold	V_{POR}	V_{CC} Rising	3.9	4.1	4.35	V
VCC POR Hysteresis	V_{POR_Hys}		--	0.3	--	V
Soft-Start Interval	T_{SS}	FB rising from 10% to 90%	1.5	2.7	4	ms
Reference Voltage	V_{REF}		--	0.8	--	V
Output Voltage Accuracy			–0.8	--	0.8	%
Thermal Shutdown Limit			--	140	--	°C

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller							
EA Open Loop Gain		G_{EA}		--	80	--	dB
EA Bandwidth		BW		--	15	--	MHz
Maximum Duty	RT8106			--	85	--	%
	RT8106A			--	80	--	%
UGATE Drive Source		$I_{UGATEsr}$		1.5	--	--	A
LGATE Drive Source		$I_{LGATEsr}$		1.5	--	--	A
UGATE Drive Sink		$R_{UGATEsk}$		--	1.1	--	Ω
LGATE Drive Sink		$R_{LGATEsk}$		--	0.65	--	Ω
Ramp Valley				--	1.6	--	V
Ramp Amplitude		ΔV_{OSC}		--	1.2	--	V
PWM Frequency	RT8106	f_{OSC}		270	300	330	kHz
	RT8106A			540	600	660	
Over Voltage Threshold		OVP	Relative to VOS	115	125	135	%
Under Voltage Threshold		UVP	Relative to VOS	65	75	80	%
PGOOD Threshold		PGOOD	Relative to VOS	90	--	110	%
OC Current Source		I_{OC}		9	10	11	μA
OC Preset Trigger Voltage		V_{OC_Preset}	R_{OCSET} is not Connected	--	0.55	--	V
Disable Threshold		V_{DIS}		--	--	0.5	V
PGOOD Active Threshold			Relative to VOS Rising	85	--	95	%
			Relative to VOS Falling	105	--	115	%
PGOOD Low Level		V_{OL_PGOOD}	Sink 4mA	--	--	0.4	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

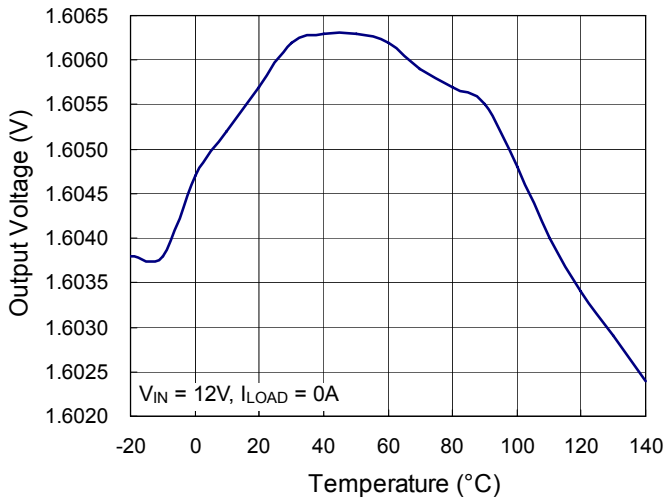
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard. The case point of θ_{JC} is on the expose pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

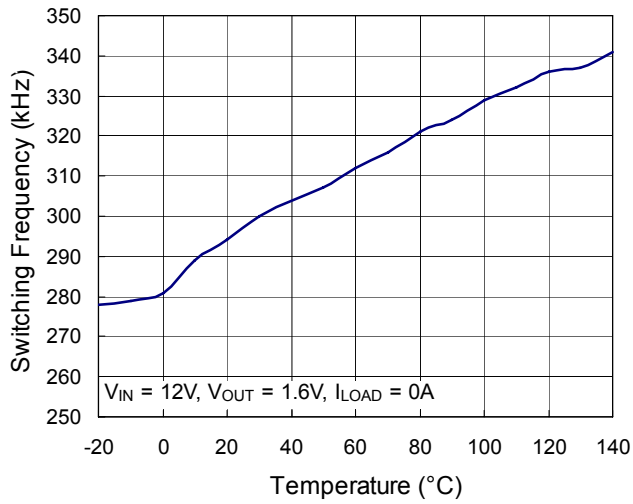
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

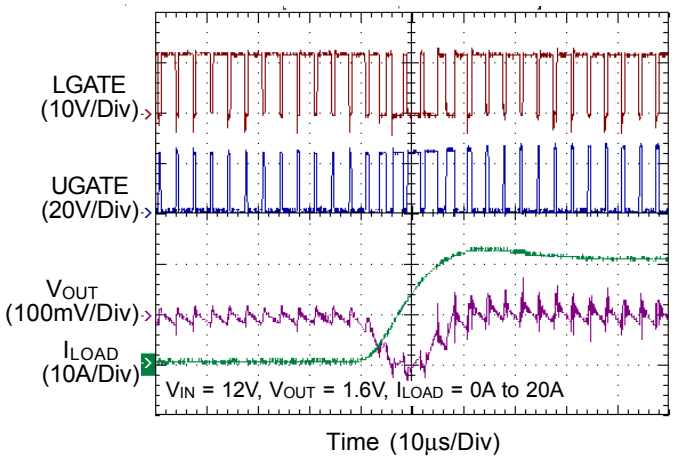
Output Voltage vs. Temperature



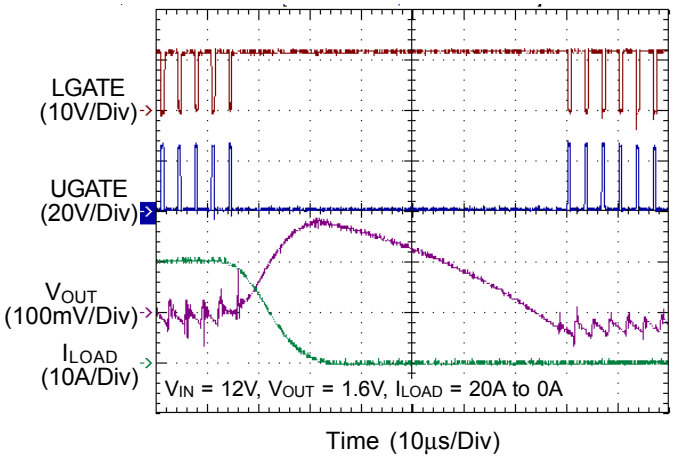
Switching Frequency vs. Temperature



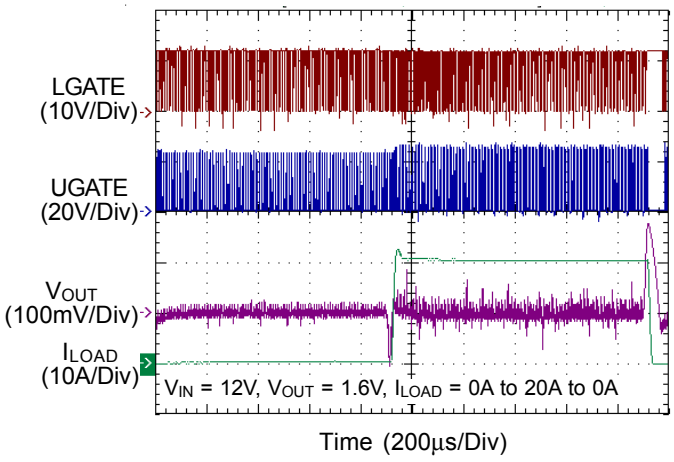
Load Transient Response



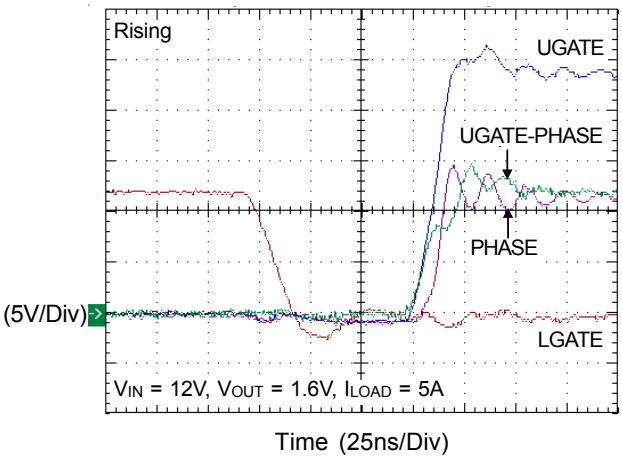
Load Transient Response



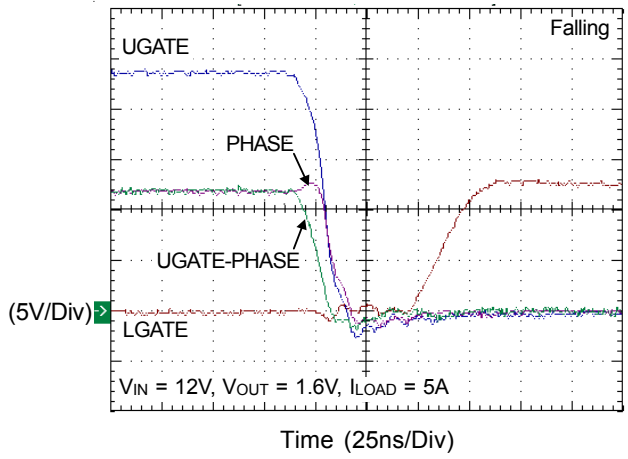
Load Transient Response



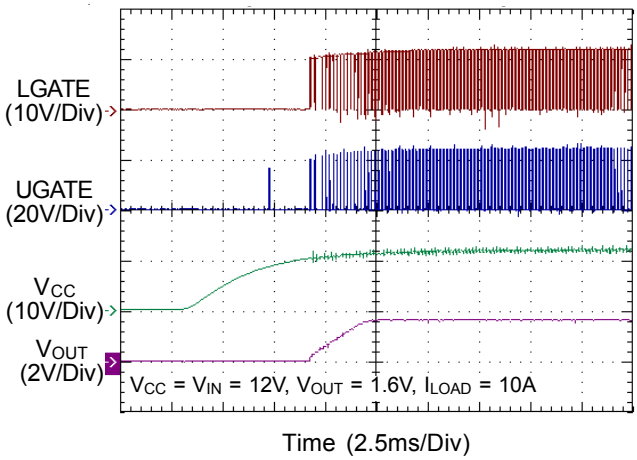
Dead Time



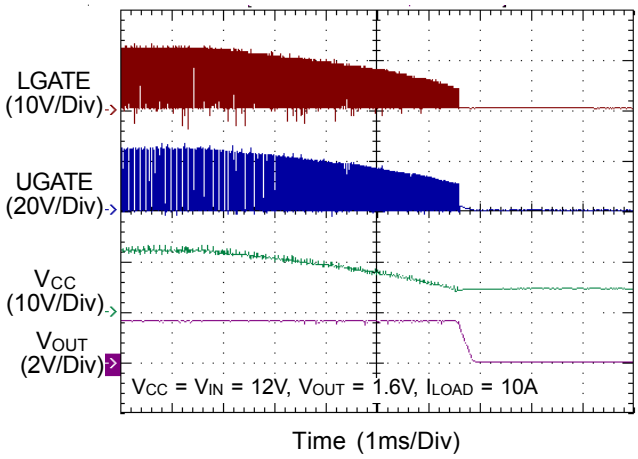
Dead Time



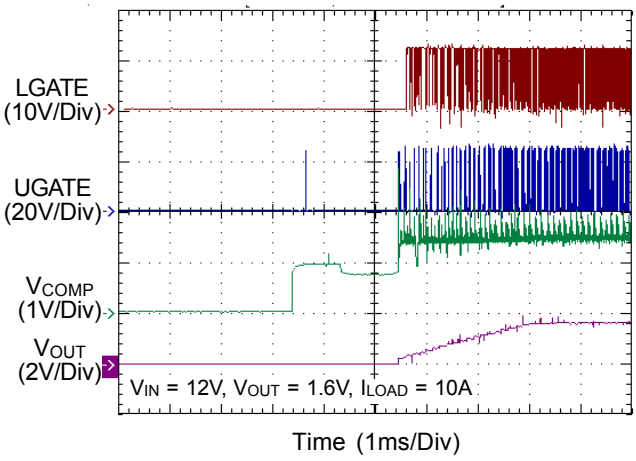
VIN = VCC Power On



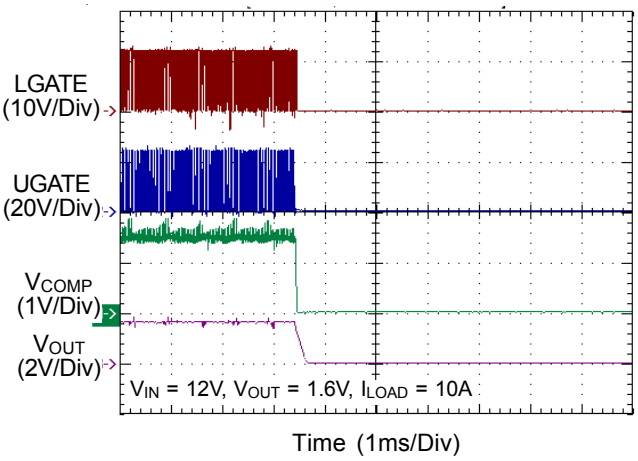
VIN = VCC Power Off



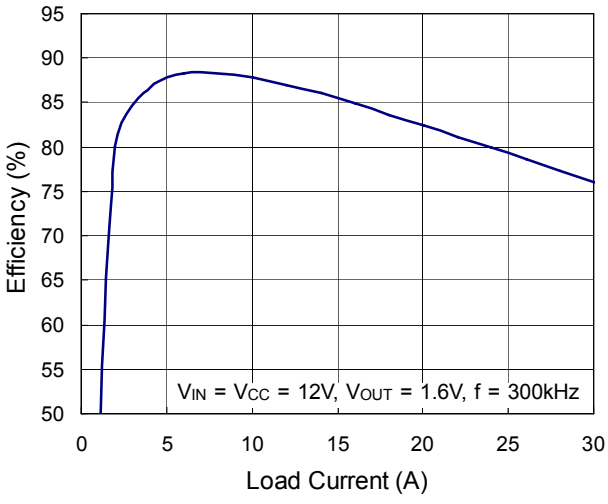
COMP Enable Power On



COMP Disable Power Off



Efficiency vs. Load Current



Application Information

Overview

The RT8106/A is a high efficiency synchronous buck PWM controller that can generate adjustable DC output voltage. This device is embedded with high current High Side and Low Side MOSFET drivers, and many protection functions (OCP, UVP, OVP) into a tiny package. Simple board design and low BOM cost can be easily achieved by the high integration feature to make this part to be an ideal solution for general applications.

Chip Enable/Disable

Pull pin 7 (COMP/EN) to be lower than 0.5V can shut down the device. This allows flexible power sequence control for specified application. Setting free this pin can enable the RT8106/A again.

Power On Reset (POR)

The RT8106/A automatically initializes upon applying of input power (at the V_{CC}) pin. The power on reset function (POR) continually monitors the V_{CC} supply voltage. The POR threshold is typically 4.1V at V_{CC} rising.

Input Power (Vin) Detection

The RT8106/A continuously generates a 10kHz pulse train with 1us pulse width to turn on the upper MOSFET for detecting the existence of V_{IN} after V_{CC} POR and Comp/EN pin enabled. As shown in Figure 1. the LX pin voltage is monitored during the detection period. If the LX pin voltage exceeds 1.5V threshold for four times, the V_{IN} existence is recognized and the RT8106/A initiates its soft start cycle.

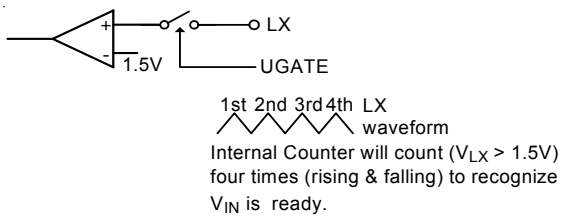


Figure 1. V_{IN} Power Detection

Soft Start

A built-in soft-start is used to prevent surge current from V_{IN} to V_{OUT} during power on. The soft-start (SS) automatically begins once the existence of V_{IN} is detected. The internal soft-start capacitor is charged and generates a linear ramping voltage across the capacitor. This voltage clamps the feedback voltage at the FB pin, causing PWM pulse width increasing slowly to reduce the output surge current. The soft-start cycle stops while the voltage across SS capacitor is higher than the nominal feedback voltage 0.8V.

Output Voltage Setting

The RT8106/A can regulate an output voltage as low to as 0.8V and maintains it within ±0.8% accuracy. Higher output voltage can be achieved by adding an offset resistor R_{OFFSET} between FB pin and GND. The steady state output voltage will be set as the formula :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB}}{R_{OFFSET}}\right)$$

Under Voltage Protection (UVP)

The VOS pin voltage is monitored for under voltage protection after soft-start completes. If the VOS voltage drops to below UV threshold (typically 75% x V_{REF}), the UVP is triggered and the RT8106/A turns off High Side and Low Side gate drivers. The RT8106/A will not be released from this latch condition unless V_{CC} POR is recognized.

Over Voltage Protection (OVP)

The VOS pin is also acted as over voltage detection after POR. If the VOS voltage rises above OVP threshold (typically 125% x V_{REF}), OVP is triggered. The RT8106/A turns off High Side gatedriver and turns Low Side gate drivers always on. The Low Side gate driver will not be turned off until VOS falls below 0.4V. The RT8106/A will not be released from this latch condition unless V_{CC} POR is recognized.

PGOOD

The RT8106/A will assert PGOOD signal after the soft-start completes and the VOS voltage is within power good range. If VOS voltage runs outside of the range, the RT8106/A de-asserts the PGOOD signal but continues switching and regulating. The PGOOD is an open drain output pin and thus requires an external pull-up resistor.

Over Current Protection

While the High Side MOSFET is off and Low Side on, the output current (I_{OUT}) flowing through the Low Side MOSFET results in a negative voltage drop (I_{OUT} x MOSFET $R_{DS(ON)}$) between the LX pin and GND. The RT8106/A senses I_{OUT} by monitoring the LX pin voltage. The maximum current is set by adjusting an external resistor R_{OCSET} connecting between LGATE and GND. The OCP is triggered if the LX voltage is lower than the LGATE voltage when low side MOSFET conducting. Because there is an internal current source 10uA flowing from the RT8106/A to the R_{OCSET}, the maximum current (I_{MAX}) can be easily derived from below equation :

$$I_{MAX} \times R_{DS(ON)} = R_{OCSET} \times 10\mu A$$

In case R_{OCSET} is not connected, RT8106/A can detect this condition and set the OC trigger voltage to a preset value (typ. 0.55V).

When the OCP is triggered, the RT8106/A will turn off both UGATE and LGATE drivers and latches in the condition unless V_{CC} POR is recognized.

Pre-Bias Start Up

In order to prevent any potential negative spike on V_{OUT} during start-up, the RT8106/A performs a special UGATE/ LGATE warm-up sequence. The UGATE keeps normal switching but the LGATE will turn on with a short pulse train instead of turning on for a long period. The Figure 2. shows that V_{OUT} rises from its initial value and no negative undershoot will happen.

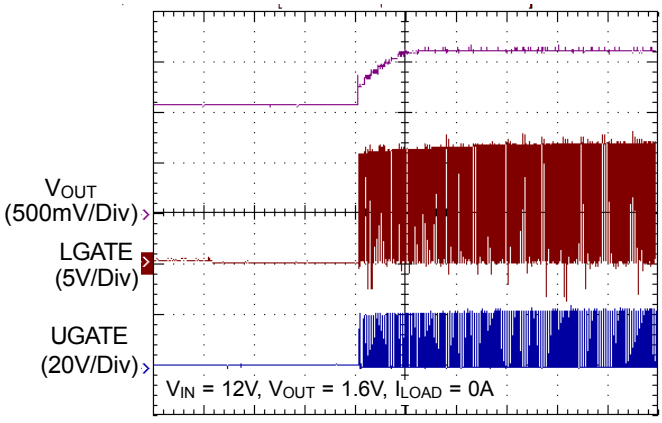


Figure 2. Pre-Bias Function

Feedback Compensation

The RT8106/A is a voltage mode controller. The control loop is a single voltage feedback path including a compensator and a modulator as shown in Figure 3. The modulator consists of the PWM comparator and power stage. The PWM comparator compares error amplifier EA output (COMP) with oscillator (OSC) sawtooth wave to provide a pulse-width modulated (PWM) with an amplitude of VIN at the LX node. The PWM wave is smoothed by the output filter L_{OUT} and C_{OUT}. The output voltage (V_{OUT}) is sensed and fed to the inverting input of the error amplifier.

A well-designed compensator regulates the output voltage to the reference voltage V_{REF} with fast transient response and good stability. In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (usually greater than 45 degrees) and the highest bandwidth (0dB crossing frequency). It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of -20dB/dec.

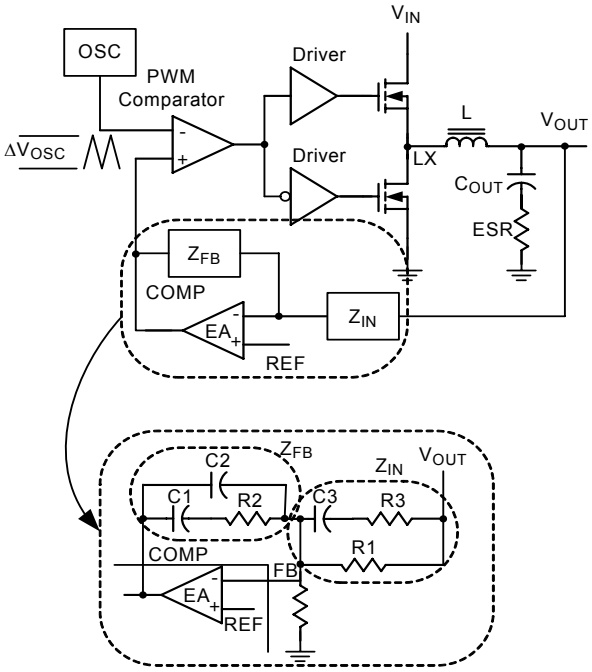


Figure 3. Closed Loop

1) Modulator Frequency Equations

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP} (output voltage over the error amplifier output). This transfer function is dominated by a DC gain, a double pole, and an ESR zero as shown in Figure 3. The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak to peak oscillator voltage V_{OSC}. The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter is expressed as :

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor is expressed as follows :

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

2) Compensation Frequency Equations

The compensation network consists of the error amplifier and the impedance networks Z_C and Z_F as shown in Figure 4.

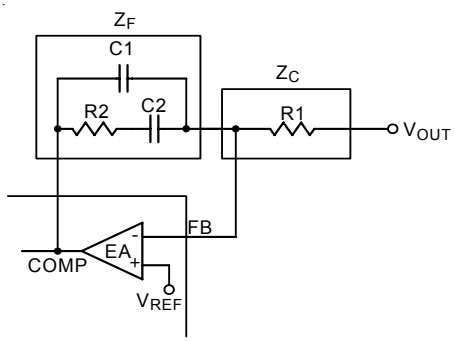


Figure 4. Compensation Loop

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}}$$

Figure 5. shows the DC-DC converter's magnitude Bode Plot. The compensation gain uses external impedance networks Z_C and Z_F to provide a stable, high bandwidth loop. High crossover frequency is desirable for fast transient response, but it often jeopardize the system stability. In order to cancel one of the LC filter poles, place the zero before the LC filter resonant frequency. In the experience, place the zero at 75% of the LC filter resonant frequency. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The second pole is placed at half the switching frequency.

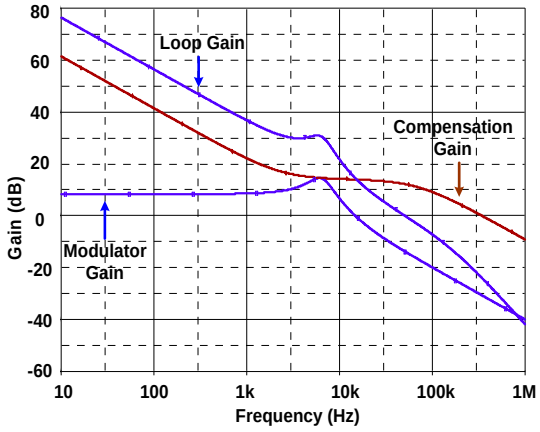
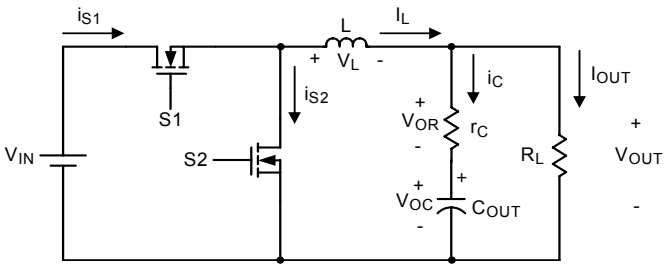


Figure 5. Bode Plot

Component Selection

1) Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. Low inductance value has smaller size, but results in low efficiency, large ripple current and high output ripple voltage. Generally, an inductor that limits the ripple current (ΔI_L) between 20% and 50% of output current is appropriate. Figure 6. shows the typical topology of the synchronous step-down converter and its related waveforms.



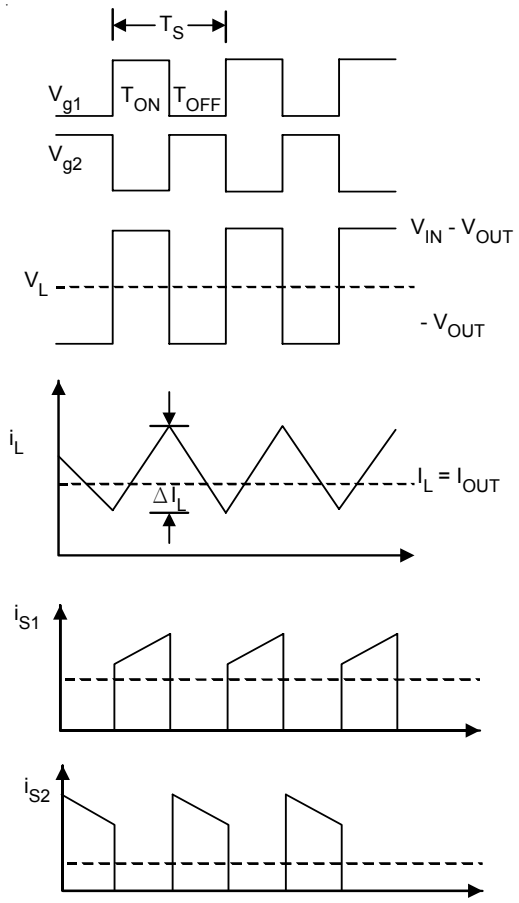


Figure 6. The Waveforms of Synchronous Step-Down Converter

According to Figure 6. the ripple current of inductor can be calculated as follows :

$$V_{IN} - V_{OUT} = L\frac{\Delta I_L}{\Delta t};\quad \Delta t = \frac{D}{fs};\quad D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times fs \times \Delta I_L} \quad (1)$$

Where :

V_{IN} = Maximum input voltage

V_{OUT} = Output Voltage

Δt = S1 turn on time

ΔI_L = Inductor current ripple

f_S = Switching frequency

D = Duty Cycle

r_C = Equivalent series resistor of output capacitor

2) Output Capacitor Selection

The selection of output capacitor depends on the output ripple voltage requirement. Practically, the output ripple voltage is a function of both capacitance value and the equivalent series resistance (ESR) r_C. Figure 7. shows the related waveforms of output capacitor.

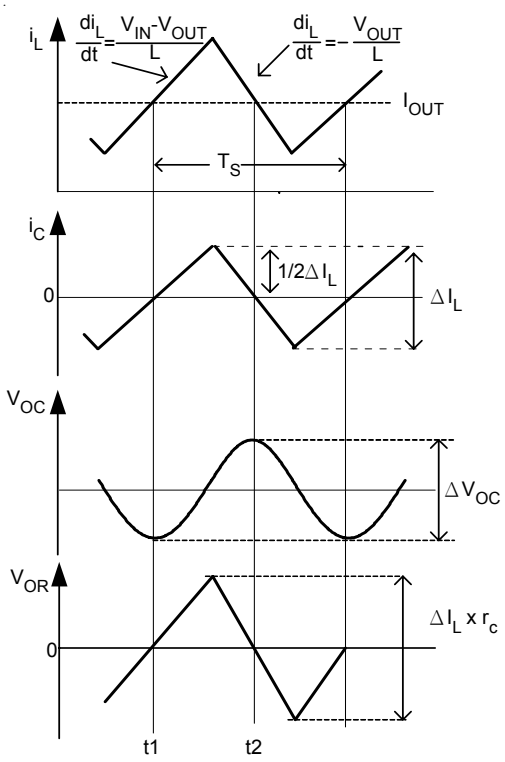


Figure 7. The Related Waveforms of Output Capacitor

The AC impedance of output capacitor at operating frequency is quite smaller than the load impedance, so the ripple current (ΔI_L) of the inductor current flows mainly through the output capacitor. The output ripple voltage is described as :

$$\Delta VOUT = \Delta VOR + \Delta VOC \quad (2)$$

$$\Delta VOUT = \Delta IL \times rc + \frac{1}{CO}\int_{t1}^{t2} ic\ dt \quad (3)$$

$$\Delta VOUT = \Delta IL \times \Delta IL \times rc + \frac{1}{8}\frac{VOUT}{COL}(1-D)T_S^2 \quad (4)$$

where ΔV_{OR} is caused by ESR and ΔV_{OC} by capacitance. For electrolytic capacitor application, typically 90% to 95% of the output voltage ripple is contributed by the ESR of the output capacitor. So Equation (4) can be simplified as: $\Delta V_{OUT} = \Delta I_L \times r_C$ (5)

Users can connect capacitors in parallel to get calculated ESR.

Input Capacitor

The selection of input capacitor is mainly based on its maximum ripple current capability. The buck converter draws pulsewise current from the input capacitor during the on time of the S1 as shown in Figure 6. The RMS value of ripple current flowing through the input capacitor is described as :

$$Irms = I_{OUT}\sqrt{D(1-D)} \quad (A) \qquad (6)$$

The input capacitor must be cable of handling this ripple current. Sometime, for higher efficiency, the low ESR capacitor is necessary.

PCB Layout Considerations

MOSFETs switch very fast and efficiently. The current transition speed between different derices causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that results in over-voltage stress on devices. Careful component placement layout and printed circuit design can minimize the voltage spikes induced in the converter. For example, during the period of upper MOSFETs turn-off transition, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET or schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes. The RT8106/A DC-DC converter integrates two sets of critical components just as follows. The switching power components are most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

For the proper layout of the RT8106/A the power components and the PWM controller should be placed firstly. And than place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near by the MOSFETs. A multi-layer printed circuit board is recommended. Figure 8 shows the connections of the critical components in the converter.

Note that the capacitors C_{IN} and C_{OUT} each of them represents numerous physical capacitors. Use a dedicated grounding plane and use vias to ground all critical components to this layer. Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the LX node, but it is not necessary to oversize this particular island. Since the LX node is subjected to very high dV/dt voltages, the stray capacitance formed between these islands and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal routing. The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

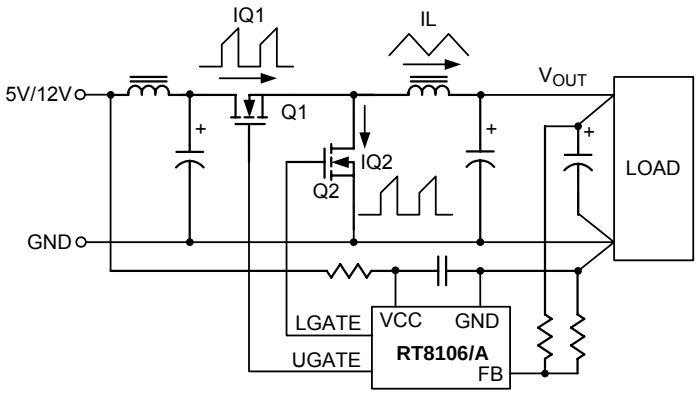


Figure 8. The Connections of the Critical Components in the Converter

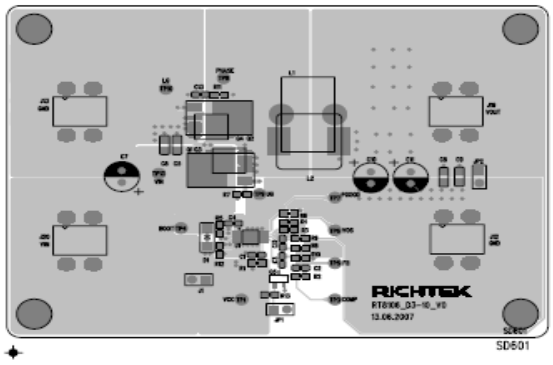


Figure 9. RT8106/A PCB (Component Side)

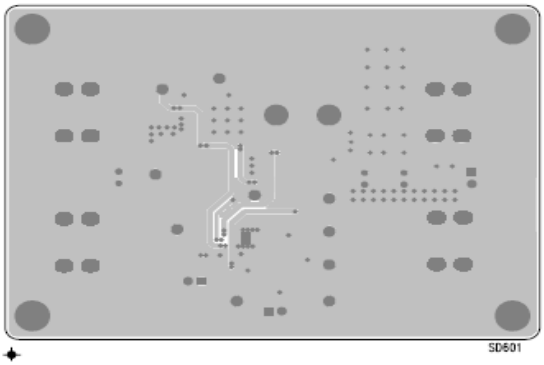
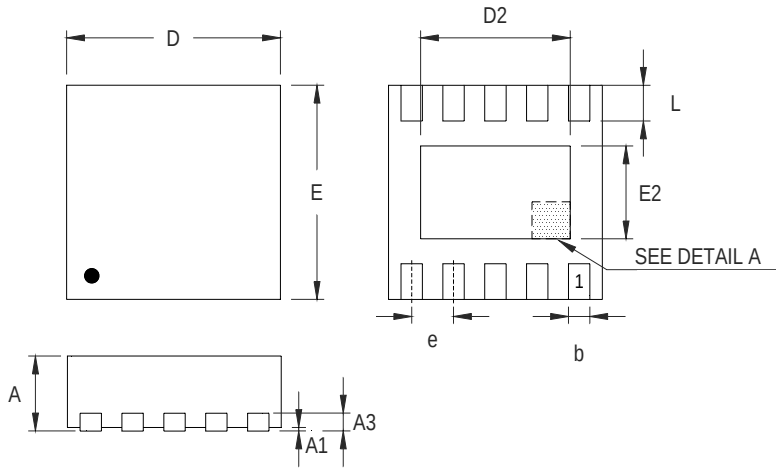
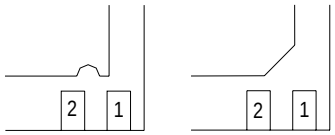


Figure 10. RT8106/A PCB (Back-Side)

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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