

# IRS21853SPBF

## DUAL HIGH SIDE DRIVER IC

### Features

- Gate drive supply range from 10 V to 20 V
- Under voltage lockout for  $V_{CC}$  &  $V_{BS1,2}$
- 5 V input logic compatible
- Tolerant to negative transient voltage
- Matched propagation delays for all channels
- RoHS compliant

### Descriptions

The IRS21853 is a high voltage, high speed power MOSFET and IGBT dual high-side driver with propagation delay matched output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The floating logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic and can be operated up to 600 V above the ground. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration, which operates up to 600 V.

### Product Summary

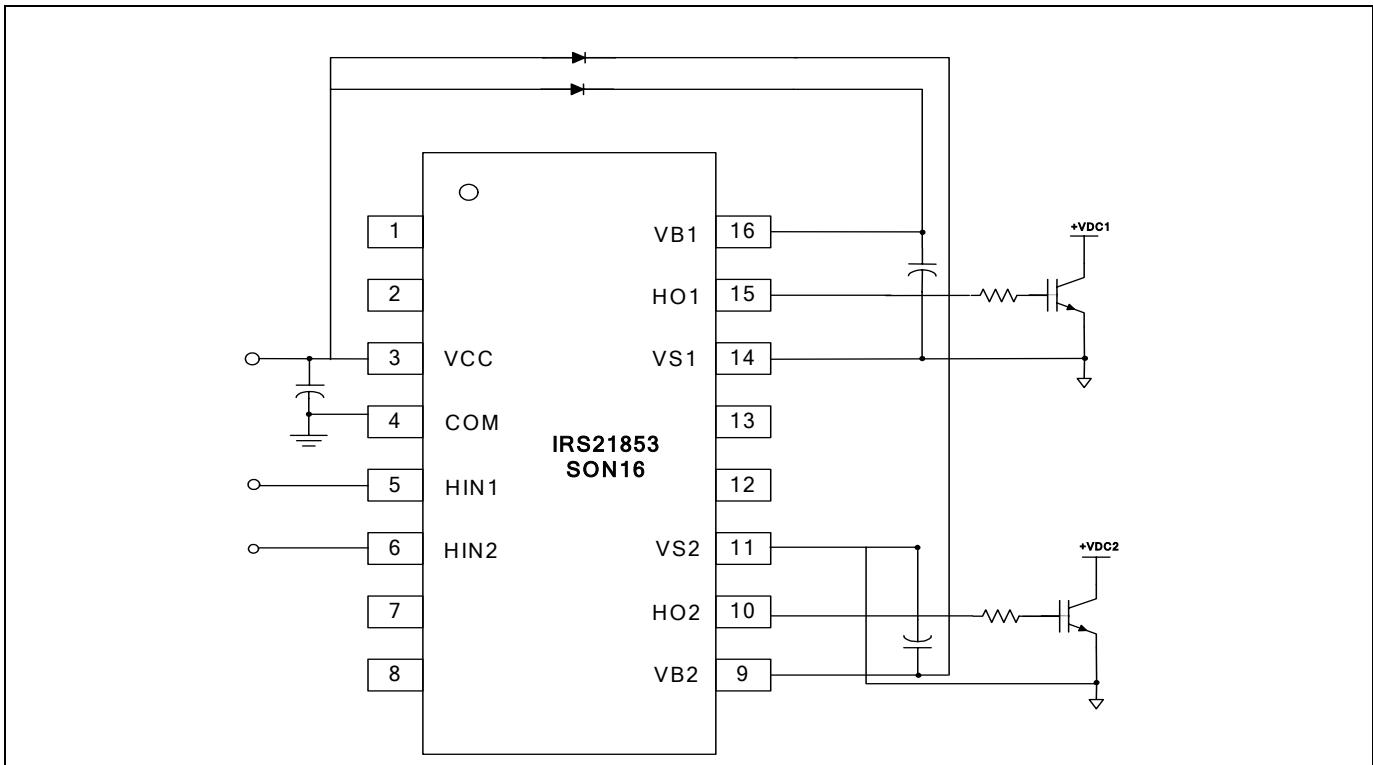
$V_{OFFSET}$	600 V max
$V_{OUT}$	10 V to 20 V
$t_{on}/t_{off}$ (typ)	170 ns/170 ns
$I_{o+/-}$	2 A/2 A
Delay Matching	40 ns

### Package

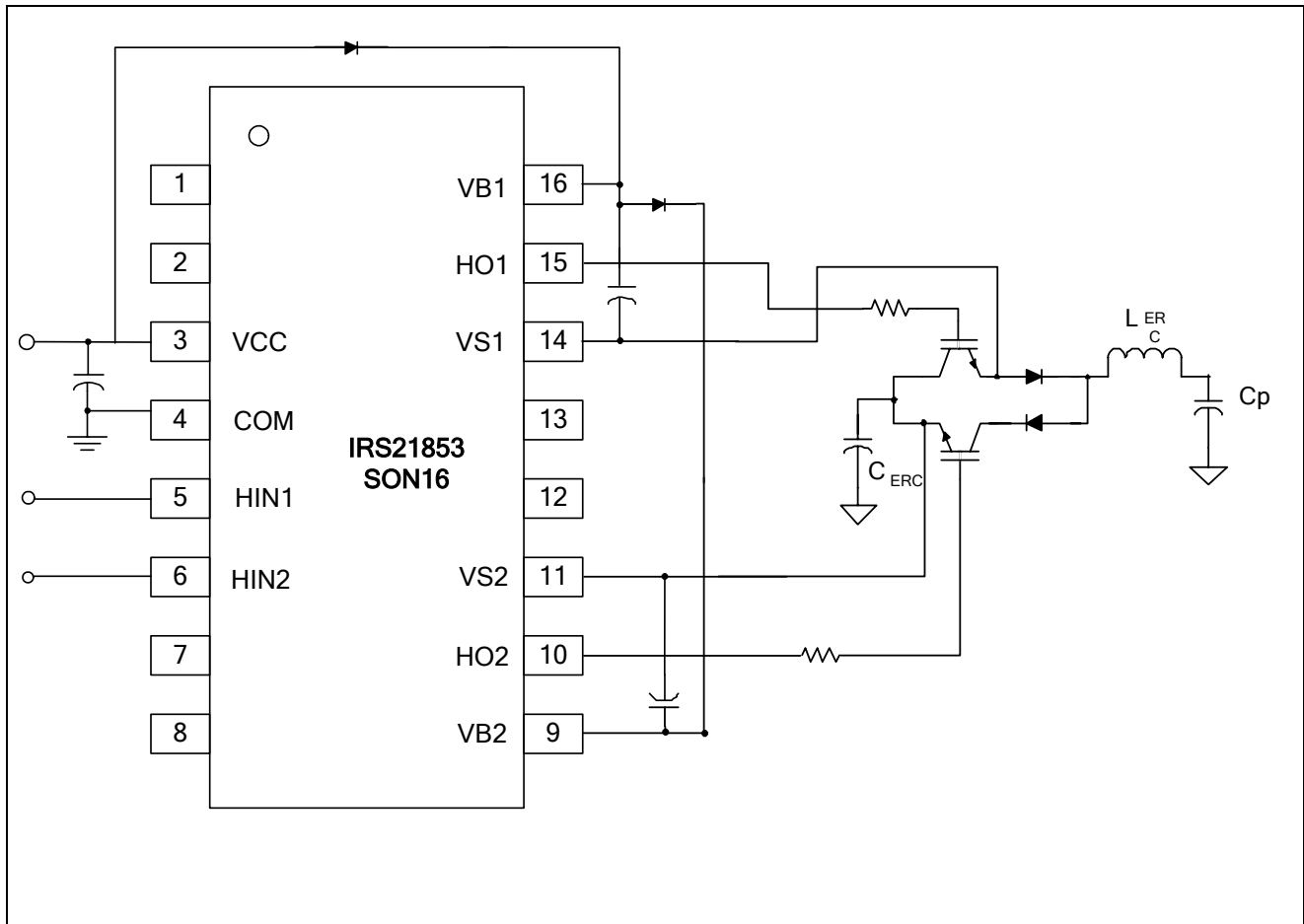


16-Lead SOIC (narrow body)

### Typical Connection Diagram



## Typical Connection Diagram for ER Circuit in PDP



### Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Symbol	Definition	Min	Max	Units
$V_{CC}$	Low side supply voltage	-0.3	20 (Note1)	V
$V_{IN}$	Logic input voltage (HIN1,2)	COM-0.3	$V_{CC}+0.3$	
$V_{B1,2}$	High side floating well supply voltage	-0.3	620 (Note1)	
$V_{S1,2}$	High side floating well supply return voltage	$V_{B1,2}-20$	$V_{Bn}+0.3$	
$V_{HO1,2}$	Floating gate drive output voltage	$V_{S1,2}-0.3$	$V_{Bn}+0.3$	
$dV_S/dt$	Allowable $V_{S1,2}$ offset supply transient relative to COM	-	50	V/ns
$P_D$	Package power dissipation @ $T_A \leq +25$ °C	-	1.25	W
$R_{\theta JA}$	Thermal resistance, junction to ambient	-	100	°C/W
$T_J$	Junction temperature	-55	150	°C
$T_S$	Storage temperature			
$T_L$	Lead temperature (soldering, 10 seconds)			
		-	300	

Note1: All supplies are fully tested at 25 V. An internal 20 V clamp exists for each supply.

### Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The offset rating are tested with supplies of  $(V_{CC}-COM)=(V_{B1,2}-V_{S1,2})=15$  V.

Symbol	Definition	Min	Max	Units
$V_{CC}$	Low side supply voltage	10	20	V
$V_{IN}$	HIN1, 2 input voltage	COM	VCC	
$V_{B1,2}$	High side floating well supply voltage	$V_{S1,2}+10$	$V_{S1,2}+20$	
$V_{S1,2}$	High side floating well supply offset voltage	Note 2	600	
$V_{HO1,2}$	Floating gate drive output voltage	$V_{S1,2}$	$V_{B1,2}$	
$T_A$	Ambient temperature	-40	125	°C

Note 2:  $V_{S1,2}$  and  $V_{B1,2}$  voltages will be tolerant to short negative transient spikes. These will be defined and specified in the future.

Note 3: Logic operation for  $V_S$  of -5 V to 600 V. Logic state held for  $V_S$  of -5 V to  $-V_{BS1,2}$ . (Please refer to Design Tip DT97-3 for more details).

**Static Electrical Characteristics**

( $V_{CC-COM}$ )=( $V_{B1,2}$ - $V_{S1,2}$ )=15 V.  $T_A = 25\text{ }^\circ\text{C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{IN,TH}$ , and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to respective  $V_{S1,2}$  and are applicable to the respective output leads HO1,2. The  $V_{CCUV}$  parameters are referenced to COM. The  $V_{BSUV1,2}$  parameters are referenced to  $V_{S1,2}$ .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions	
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	8.0	8.9	9.8	V		
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.4	8.2	9.0			
$V_{BSUV+}$	$V_{BS1,2}$ supply undervoltage positive going threshold	8.0	8.9	9.8			
$V_{BSUV-}$	$V_{BS1,2}$ supply undervoltage negative going threshold	7.4	8.2	9.0			
$I_{LK1,2}$	High-side floating well offset supply leakage current	---	---	50	$\mu\text{A}$	$V_{B1,2} = V_{S1,2} = 600\text{ V}$	
$I_{QBS}$	Quiescent $V_{BS}$ supply current	---	75	150		$HIN1,2 = 0\text{ V or }5\text{ V}$	
$I_{QCC}$	Quiescent $V_{CC}$ supply current	---	110	220			
$V_{IH}$	Logic "1" input voltage	3.5	---	---	V		
$V_{IL}$	Logic "0" input voltage	---	---	0.6			
$V_{OH}$	HO1,2 high level output voltage, $V_{BIAS}-V_O$	---	---	1.4			$I_o = 0\text{ A}$
$V_{OL}$	HO1,2 low level output voltage, $V_O$	---	---	0.0 6			$I_o = 20\text{ mA}$
$I_{IN+}$	Logic "1" input bias current	---	5	20	$\mu\text{A}$	$V_{HIN1,2} = 5\text{ V}$	
$I_{IN-}$	Logic "0" input bias current	---	---	5		$V_{HIN1,2} = 0\text{ V}$	
$I_{O+}$	Output high short circuit pulsed current HO1,2	---	2	---	A	$V_O = 0\text{ V}, V_{IN} = 0\text{ V}, PW \leq 10\text{ }\mu\text{s}$	
$I_{O-}$	Output low short circuit pulsed current HO1,2	---	2	---		$V_O = 15\text{ V}, V_{IN} = 5\text{ V}, PW \leq 10\text{ }\mu\text{s}$	

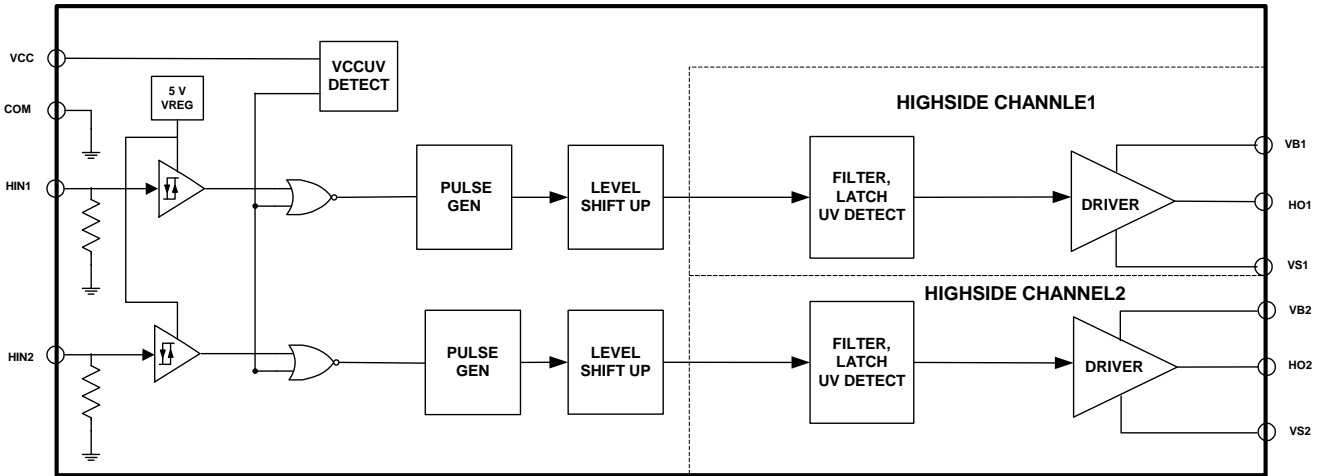
**Dynamic Electrical Characteristics (All values are target data)**

( $V_{CC-COM}$ ) = ( $V_{B1,2}-V_{S1,2}$ ) = 15 V.  $T_A$  = 25 °C unless otherwise specified.  $C_L$  = 1000 pF unless otherwise specified. All parameters are reference to COM.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
$t_{on}$	Turn-on propagation delay (HO1,2)	---	170	---	ns	( $V_{S1,2-COM}$ ) = 0 V
$t_{off}$	Turn-off propagation delay (HO1,2)	---	170	---		( $V_{S1,2-COM}$ ) = 600 V
$t_r$	Turn-on rise time	---	15	50		
$t_f$	Turn-off fall time	---	15	50		
MT	Delay matching (Note 1)	---	---	40		

Note 4:  $\text{Max}(t_{on,HO1}, t_{on,HO2}) - \text{Min}(t_{on,HO1}, t_{on,HO2})$ ;  $\text{Max}(t_{off,HO1}, t_{off,HO2}) - \text{Min}(t_{off,HO1}, t_{off,HO2})$

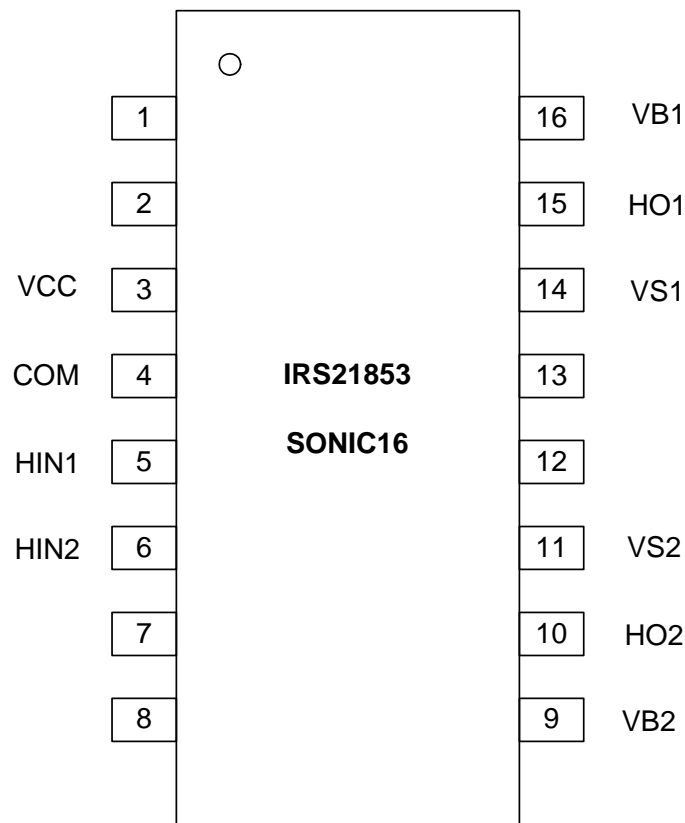
**Functional Block Diagram**

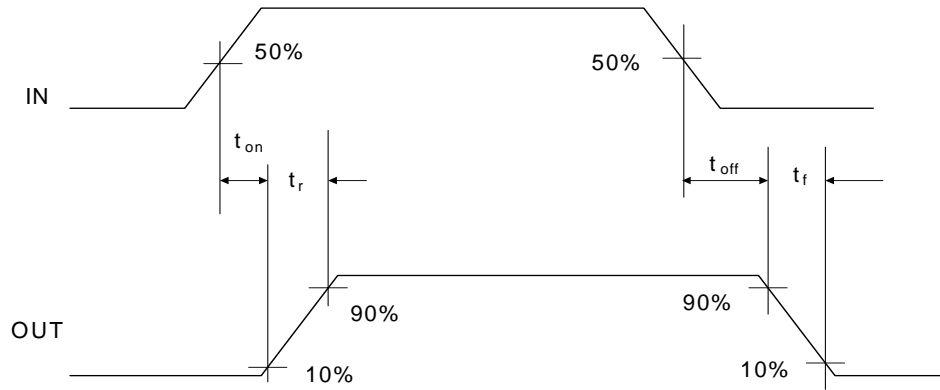


**Lead Definitions**

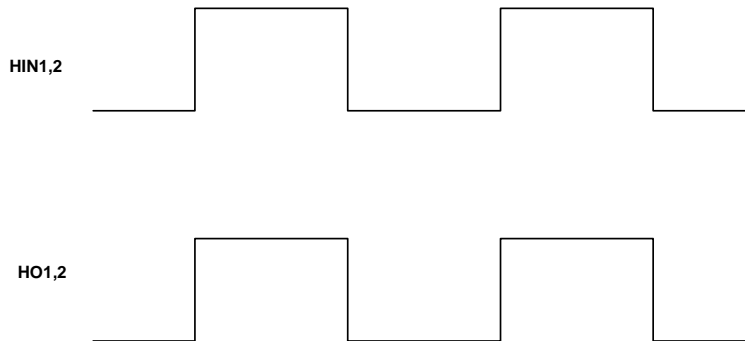
Symbol	Description
VCC	Low side supply voltage
COM	Ground
VB1,2	High side gate drive floating supply
HO1,2	High side driver outputs
VS1,2	High voltage floating supply return
HIN1,2	Logic inputs for high side gate driver outputs (in phase)

**Lead Assignments**



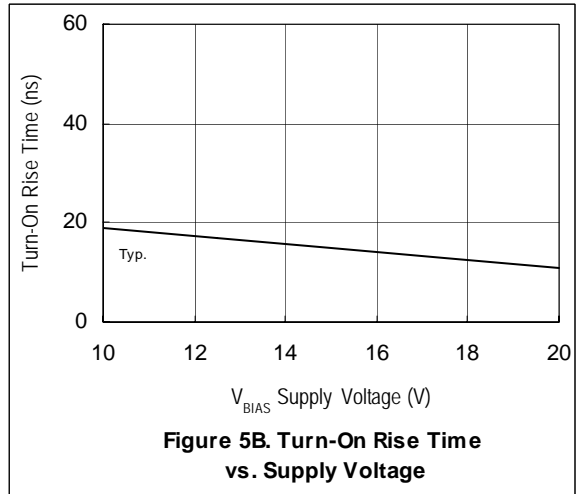
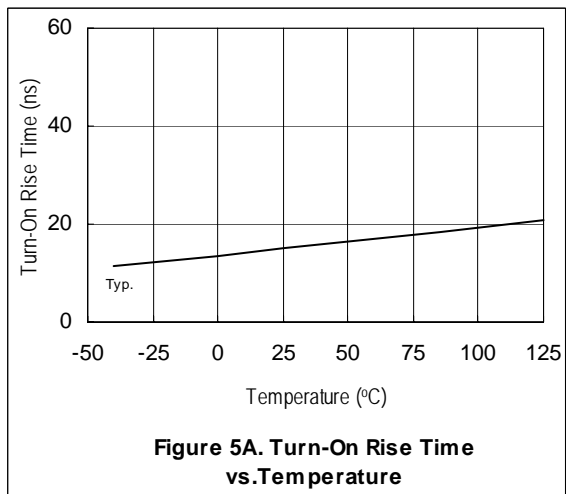
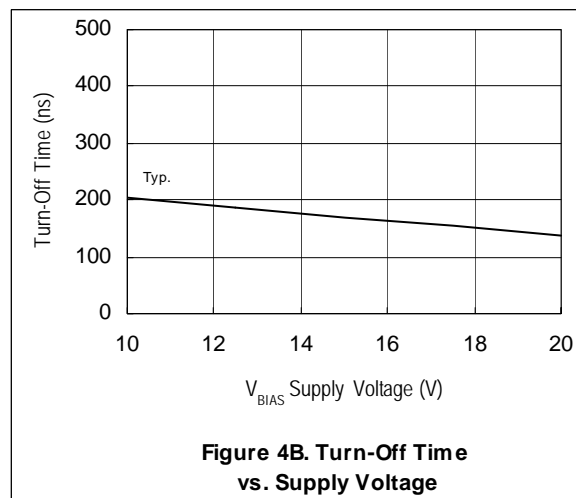
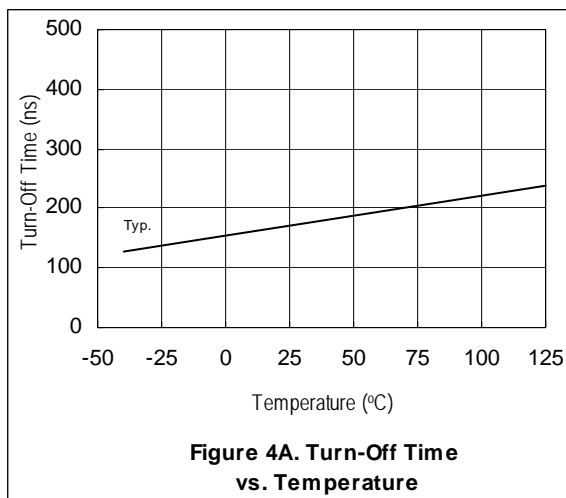
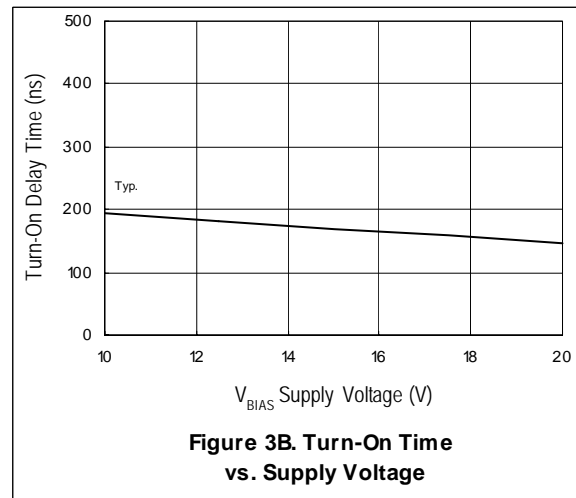
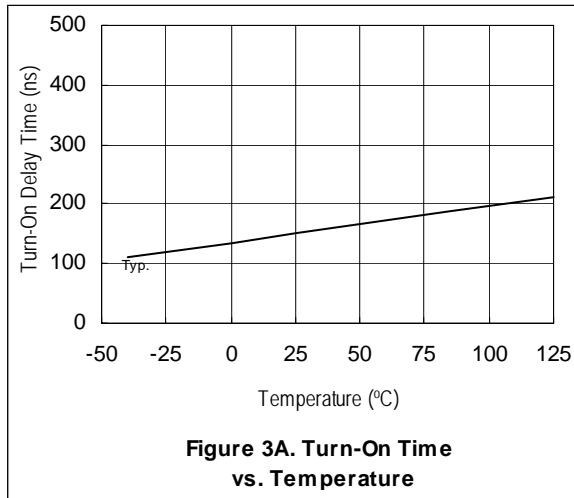


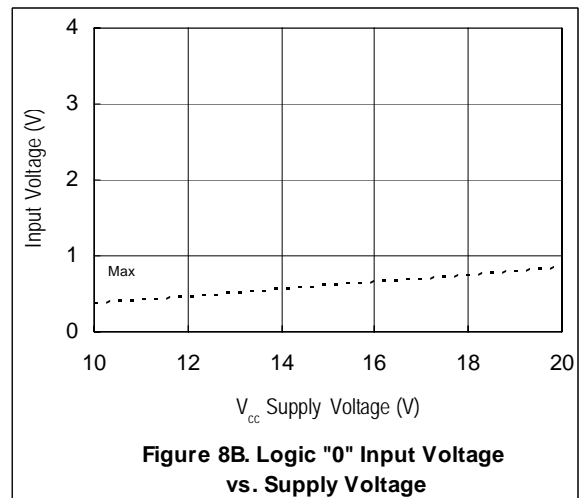
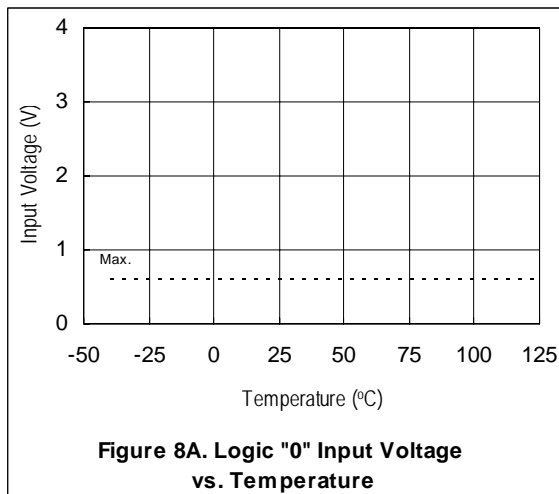
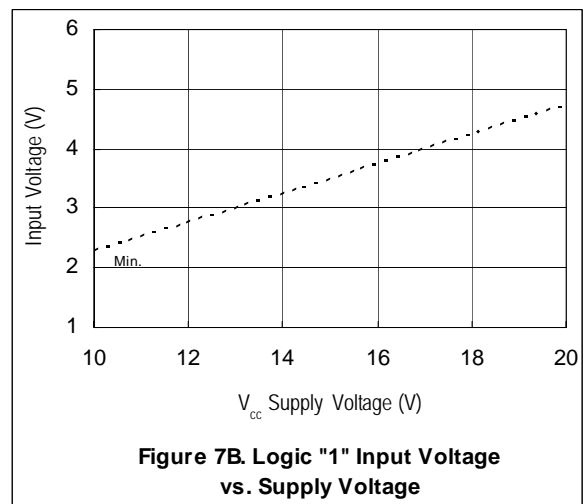
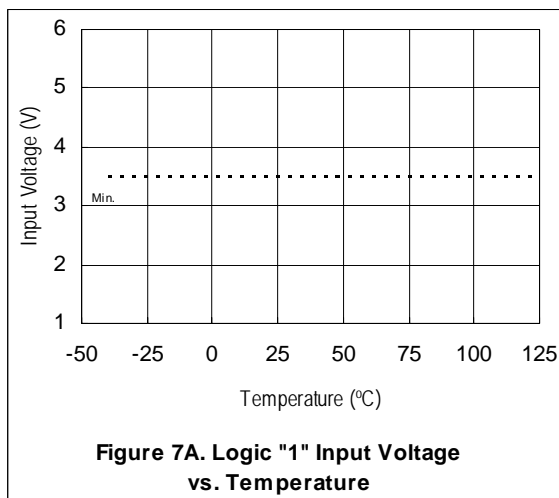
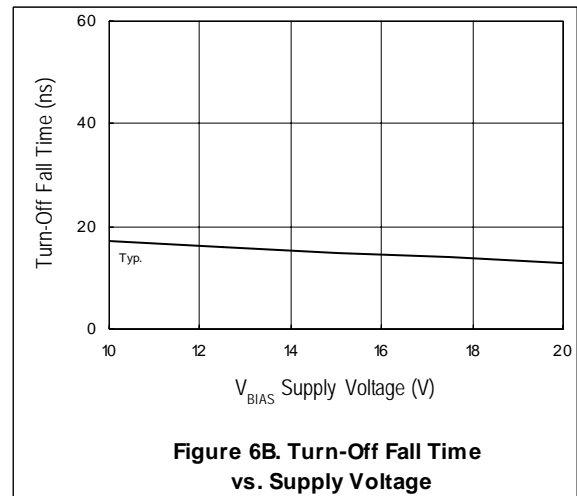
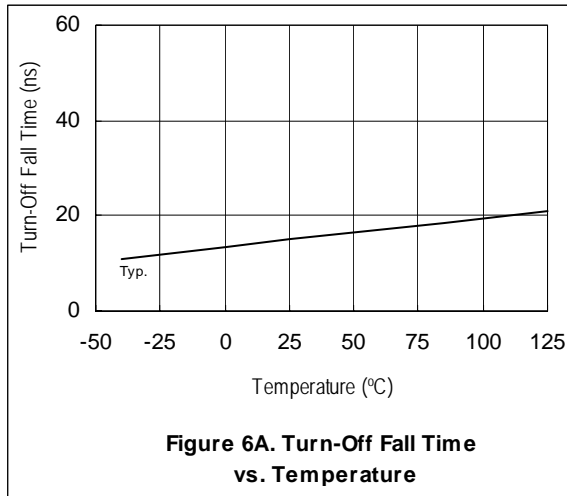
**Figure 1: Switching Time Waveforms**

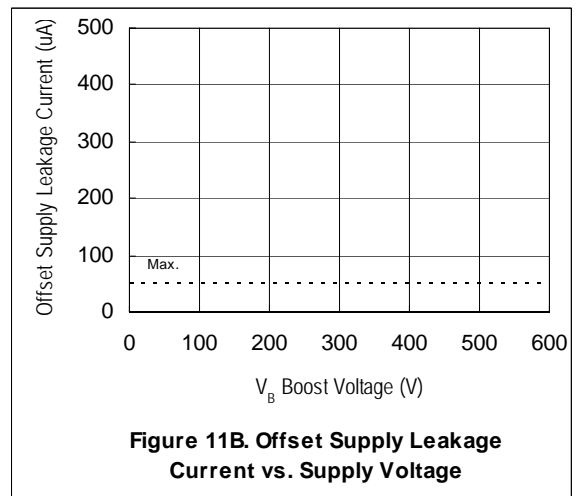
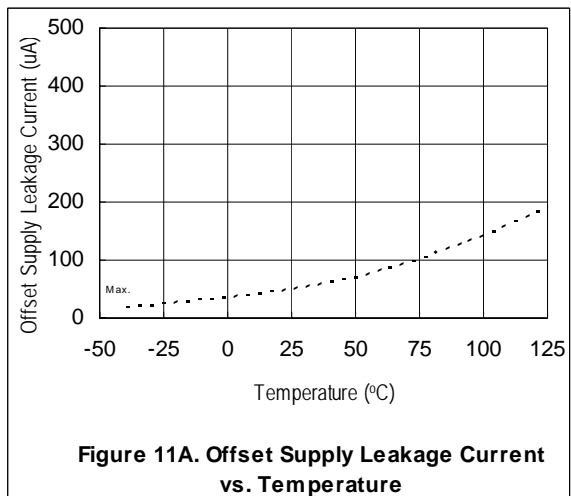
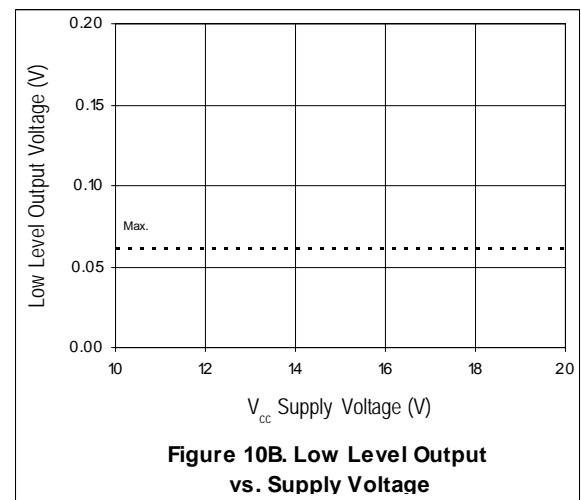
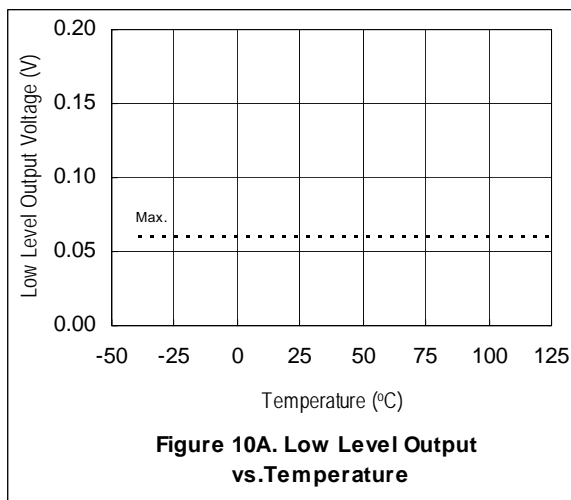
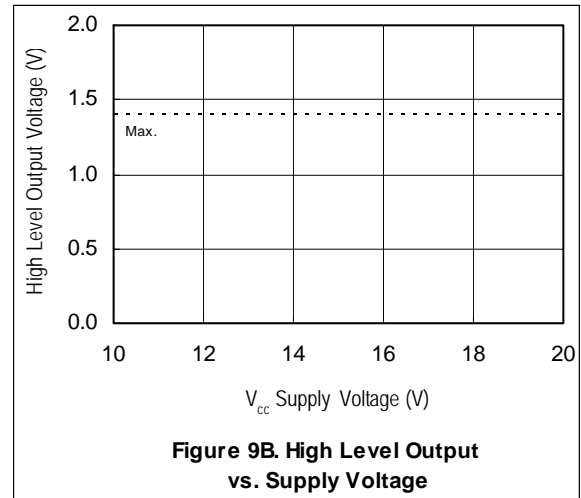
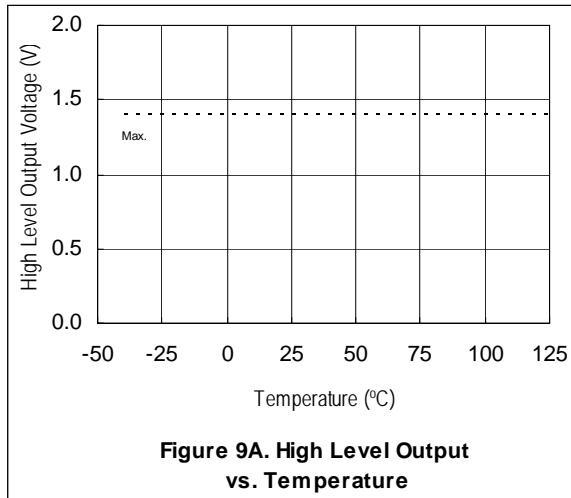


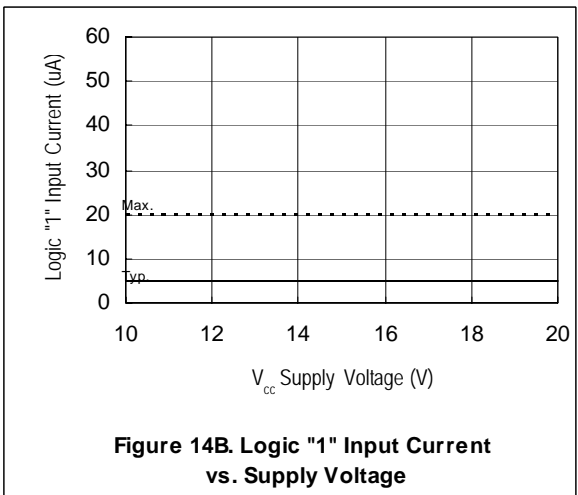
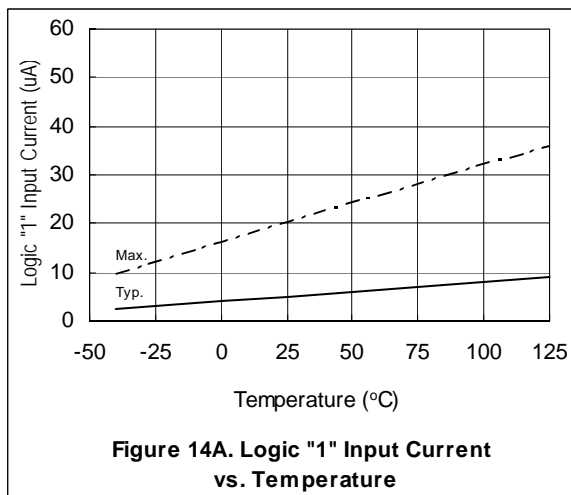
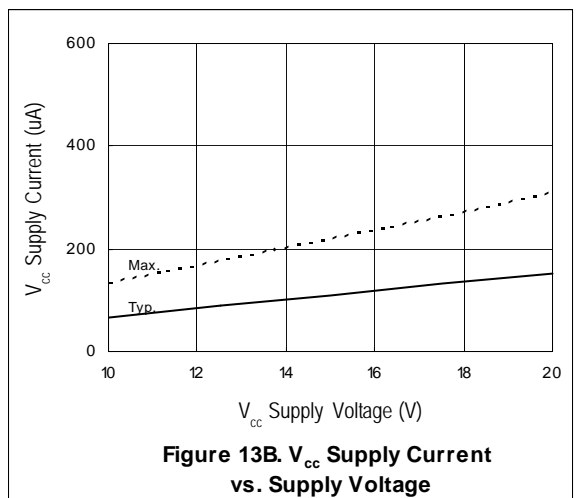
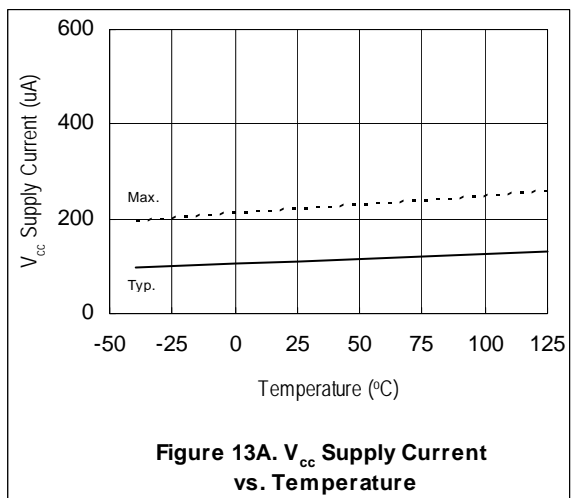
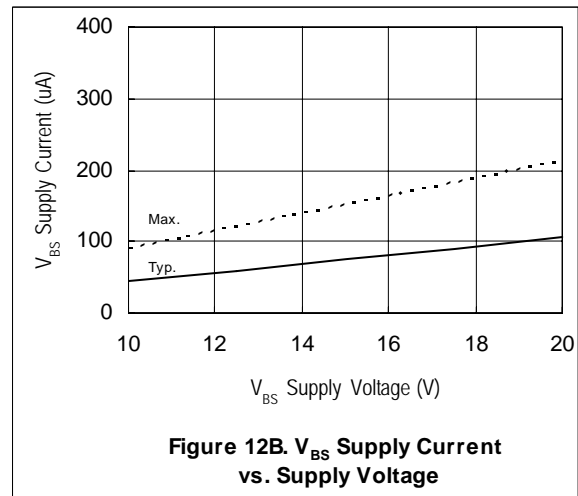
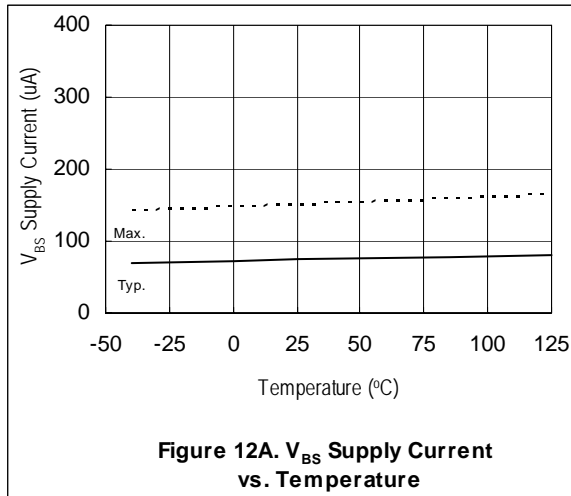
**Figure 2: Input/Output Timing Diagram**

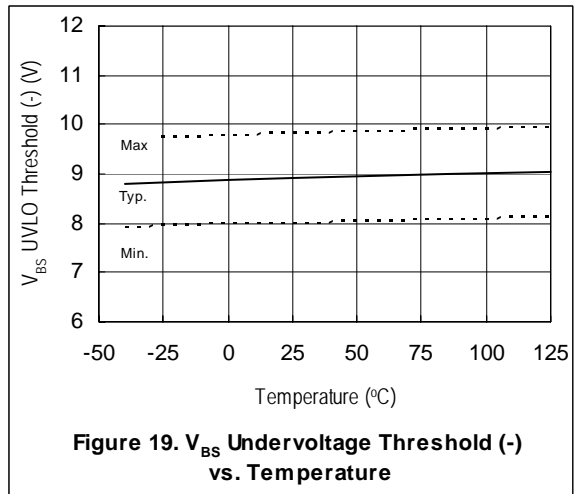
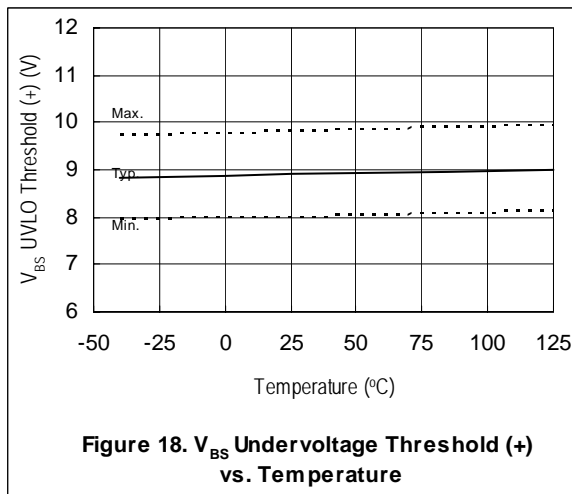
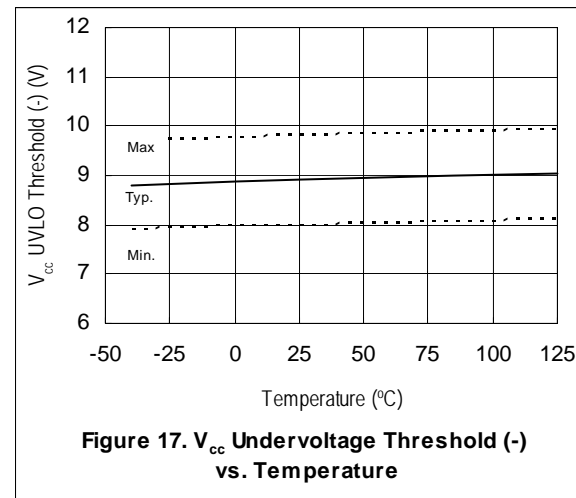
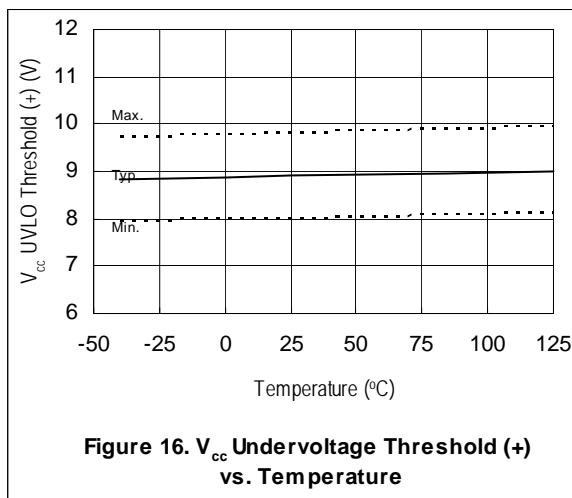
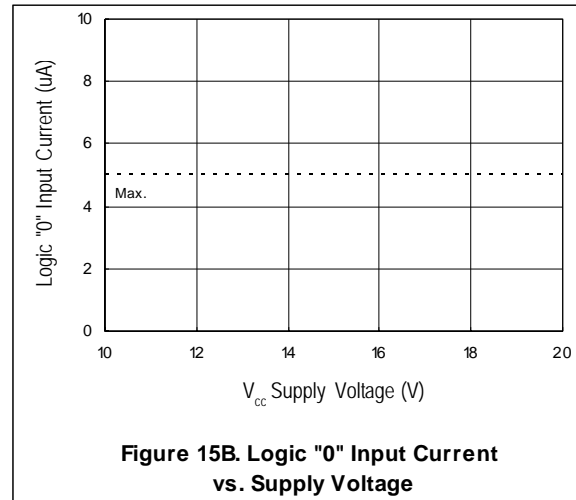
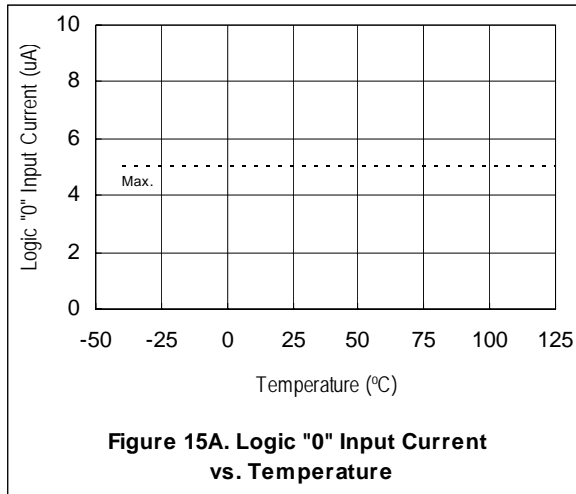


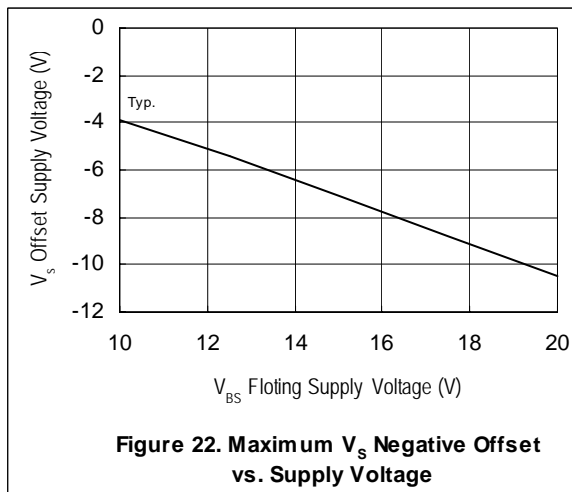
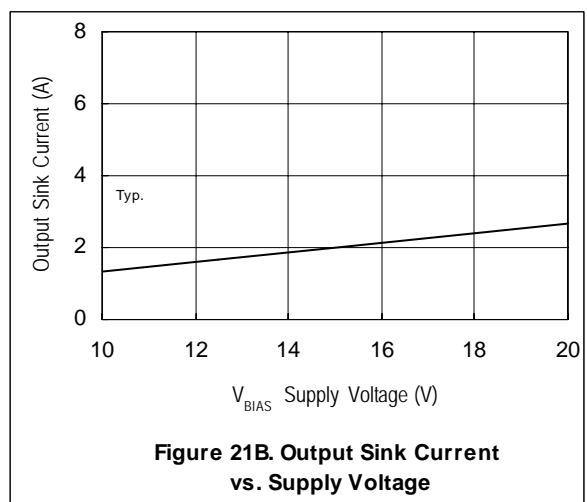
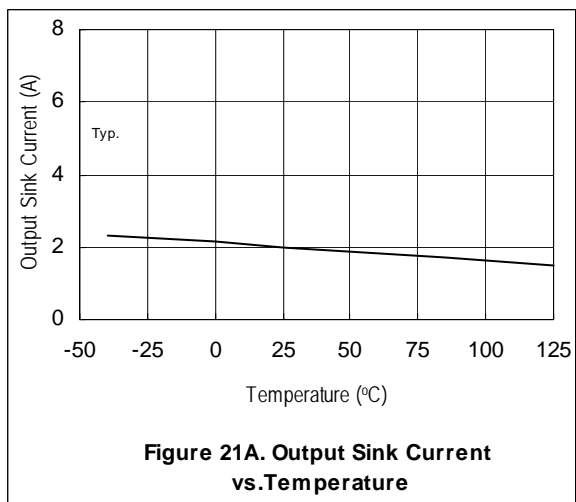
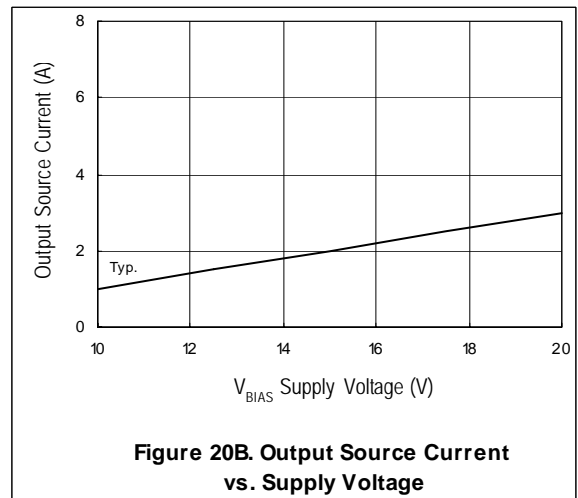
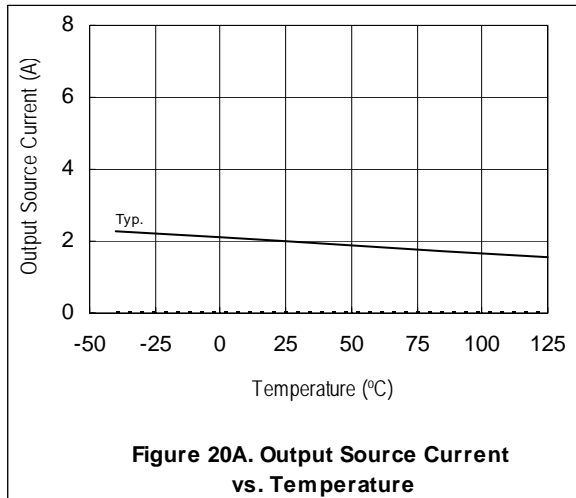


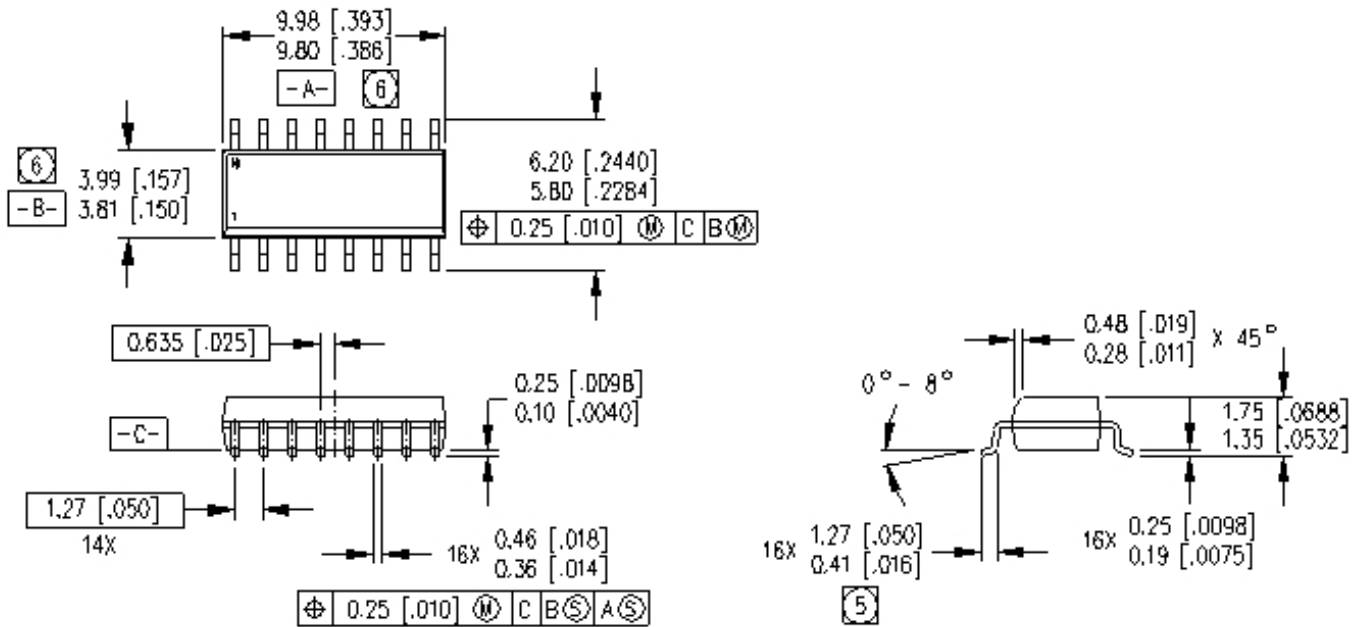








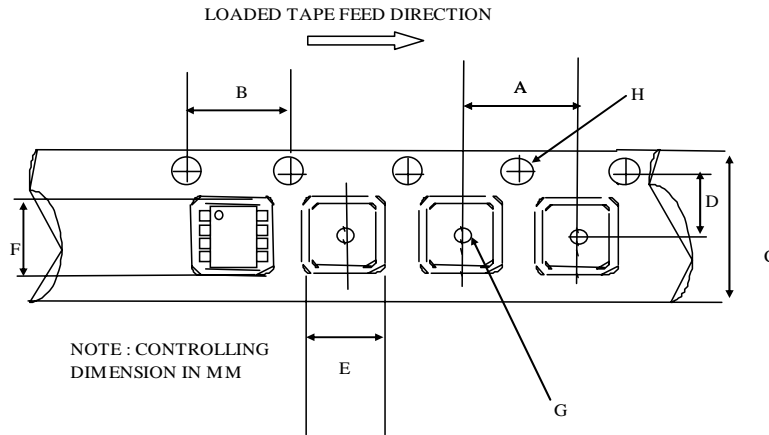




**NOTES:**

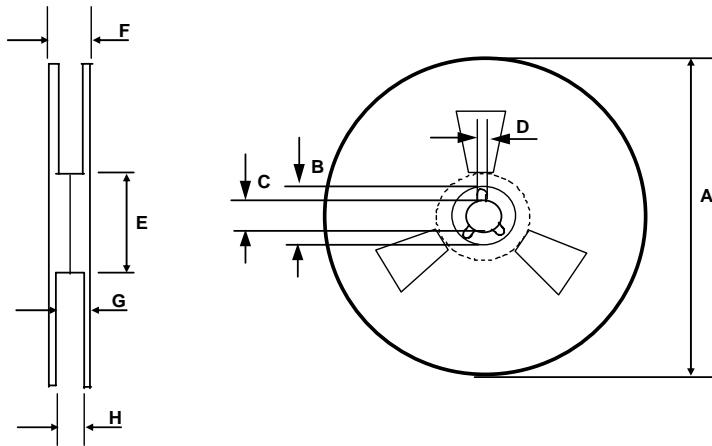
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5W-1982
2. CONTROLLING DIMENSION. MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETER [INCHES]
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006]

**16-Lead SOIC (narrow body)**



CARRIER TAPE DIMENSION FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062

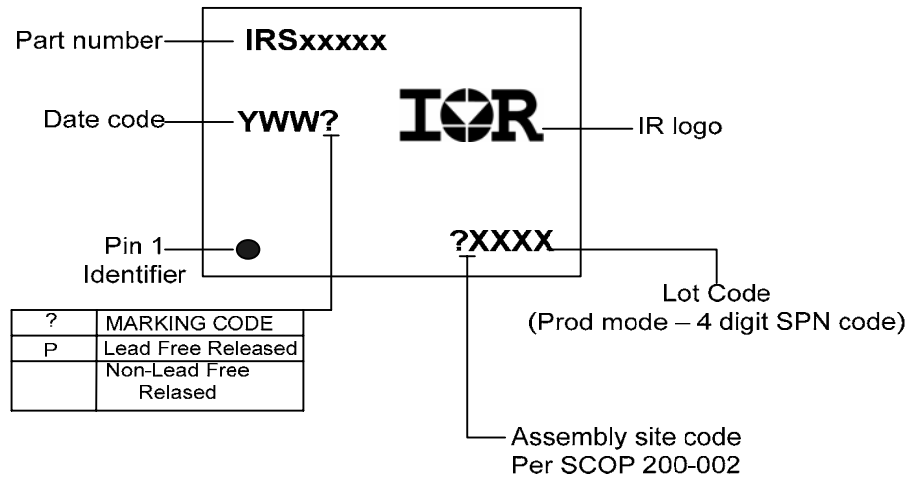


REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724



**LEAD-FREE PART MARKING INFORMATION**



**ORDER INFORMATION**

16-Lead SOIC IRS21853SPBF

16-Lead SOIC Tape & Reel IRS21853STRPBF