# CY7C1021CV33

## 1-Mbit (64K x 16) Static RAM

## Features

- Temperature ranges
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to 85°C
  - Automotive-A: –40°C to 85°C
  - Automotive-E: –40°C to 125°C
- Pin and function compatible with CY7C1021BV33
- High speed
  - $t_{AA}$ = 8 ns (Commercial & Industrial)
  - $t_{AA}$ = 12 ns (Automotive-E)
- CMOS for optimum speed and power
- Low active power: 325 mW (max)
- Automatic power down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin 400 Mil SOJ, 44-pin TSOP II and 48-Ball FBGA packages

## Functional Description

The CY7C1021CV33 is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

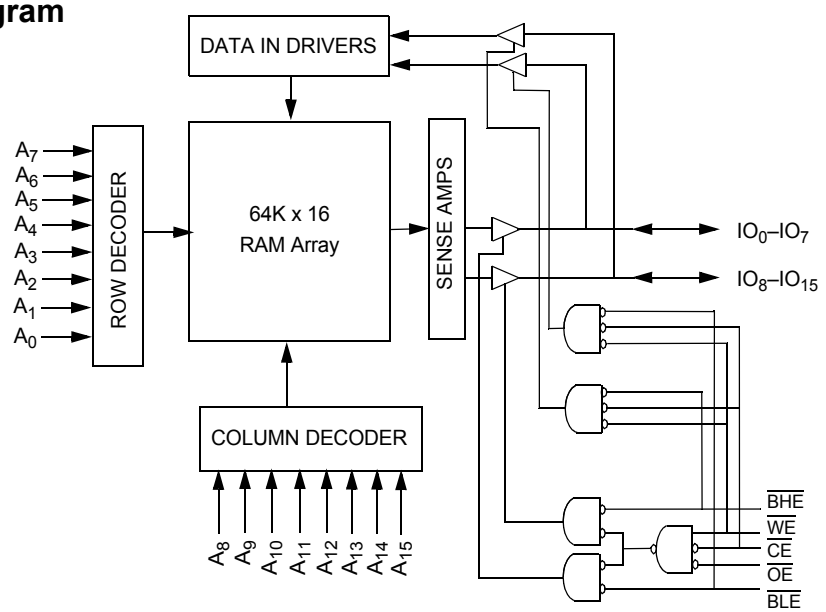
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins ($IO_1$ through $IO_8$), is written into the location specified on the address pins ($A_0$ through $A_{15}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from IO pins ($IO_9$ through $IO_{16}$) is written into the location specified on the address pins ($A_0$ through $A_{15}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on $IO_1$ to $IO_8$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on $IO_9$ to $IO_{16}$. For more information, see the "Truth Table" on page 9 for a complete description of Read and Write modes.

The input and output pins ($IO_1$ through $IO_{16}$) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

## Logic Block Diagram



## Selection Guide

| | | -8 | -10 | -12 | -15 | Unit |
|---|---|---|---|---|---|---|
| Maximum Access Time | | 8 | 10 | 12 | 15 | ns |
| Maximum Operating Current | Comm'l/Ind'l | 95 | 90 | 85 | 80 | mA |
| | Automotive-A | | | | 80 | mA |
| | Automotive-E | | | 90 | | mA |
| Maximum CMOS Standby Current | Comm'l/Ind'l | 5 | 5 | 5 | 5 | mA |
| | Automotive-A | | | | 5 | mA |
| | Automotive-E | | | 10 | | mA |

## Pin Configuration

**Figure 1. 44-Pin SOJ/TSOP II** [1]

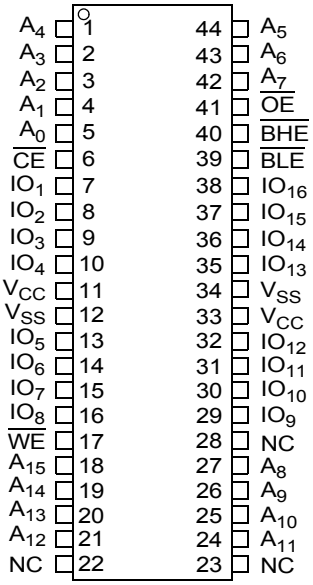
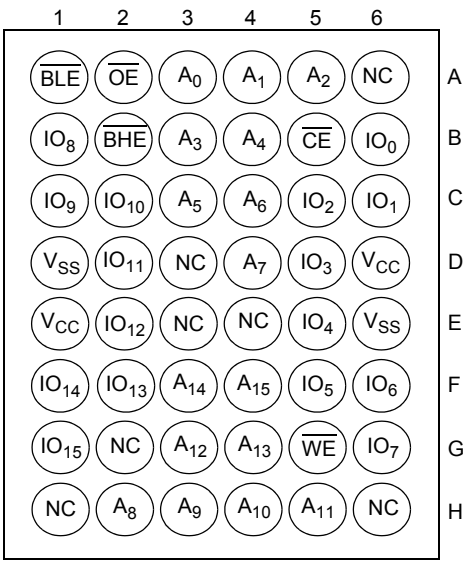



**Figure 2. 48-Ball FBGA Pinout** [1]




**Note**
1. NC pins are not connected on the die.

## Pin Definitions

| Pin Name | SOJ, TSOP Pin Number | BGA Pin Number | IO Type | Description |
|---|---|---|---|---|
| $A_0$–$A_{15}$ | 1–5, 18–21, 24–27, 42–44 | A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4 | Input | **Address Inputs.** Used to select one of the address locations. |
| $IO_1$–$IO_{16}$ [2] | 7–10, 13–16, 29–32, 35–38 | B6, C6, C5, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1 | Input or Output | **Bidirectional Data IO lines**. Used as input or output lines depending on operation. |
| NC | 22, 23, 28 | A6, D3, E3, E4, G2, H1, H6 | No Connect | **No Connects**. Not connected to the die. |
| $\overline{WE}$ | 17 | G5 | Input or Control | **Write Enable Input, Active LOW**. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted. |
| $\overline{CE}$ | 6 | B5 | Input or Control | **Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip. |
| $\overline{BHE}$, $\overline{BLE}$ | 40, 39 | B2, A1 | Input or Control | **Byte Write Select Inputs, Active LOW**. $\overline{BHE}$ controls $IO_{16}$ – $IO_9$, $\overline{BLE}$ controls $IO_8$ – $IO_1$. |
| $\overline{OE}$ | 41 | A2 | Input or Control | **Output Enable, Active LOW**. Controls the direction of the IO pins. When LOW, the IO pins are allowed to behave as outputs. When deasserted HIGH, the IO pins are tri-stated and act as input data pins. |
| $V_{SS}$ | 12, 34 | D1, E6 | Ground | **Ground for the device**. Connected to ground of the system. |
| $V_{CC}$ | 11, 33 | D6, E1 | Power Supply | **Power Supply Inputs to the Device.** |

**Note**
2. $IO_1$–$IO_{16}$ for SOJ/TSOP and $IO_0$–$IO_{15}$ for BGA packages.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on $V_{CC}$ Relative to GND[3].....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[3].....–0.5V to $V_{CC}$+0.5V

DC Input Voltage[3] .....–0.5V to $V_{CC}$+0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature ($T_A$) | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 3.3V ± 10% |
| Industrial | –40°C to +85°C | |
| Automotive-A | –40°C to +85°C | |
| Automotive -E | –40°C to +125°C | |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | -8 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min, $I_{OH}$ = –4.0 mA | | 2.4 | | 2.4 | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min, $I_{OL}$ = 8.0 mA | | | 0.4 | | 0.4 | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[3] | | | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | Com'l/Ind'l | –1 | +1 | –1 | +1 | –1 | +1 | –1 | +1 | µA |
| | | | Auto-A | | | | | | | –1 | +1 | |
| | | | Auto-E | | | | | –12 | +12 | | | |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$, Output disabled | Com'l/Ind'l | –1 | +1 | –1 | +1 | –1 | +1 | –1 | +1 | µA |
| | | | Auto-A | | | | | | | –1 | +1 | |
| | | | Auto-E | | | | | –12 | +12 | | | |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | Com'l/Ind'l | | 95 | | 90 | | 85 | | 80 | mA |
| | | | Auto-A | | | | | | | | 80 | |
| | | | Auto-E | | | | | | 90 | | | |
| $I_{SB1}$ | Automatic CE Power Down Current —TTL Inputs | Max $V_{CC}$, $\overline{CE}$ ≥ $V_{IH}$ $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | Com'l/Ind'l | | 15 | | 15 | | 15 | | 15 | mA |
| | | | Auto-A | | | | | | | | 15 | |
| | | | Auto-E | | | | | | 20 | | | |
| $I_{SB2}$ | Automatic CE Power Down Current — CMOS Inputs | Max $V_{CC}$, $\overline{CE}$ ≥ $V_{CC}$ – 0.3V, $V_{IN}$ ≥ $V_{CC}$ – 0.3V, or $V_{IN}$ ≤ 0.3V, f = 0 | Com'l/Ind'l | | 5 | | 5 | | 5 | | 5 | mA |
| | | | Auto-A | | | | | | | | 5 | |
| | | | Auto-E | | | | | | 10 | | | |

**Note**

3. $V_{IL}$ (min) = –2.0V and $V_{IH}$(max) = $V_{CC}$ + 0.5V for pulse durations of less than 20 ns.

## Capacitance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 8 | pF |
| $C_{OUT}$ | Output Capacitance | | 8 | pF |

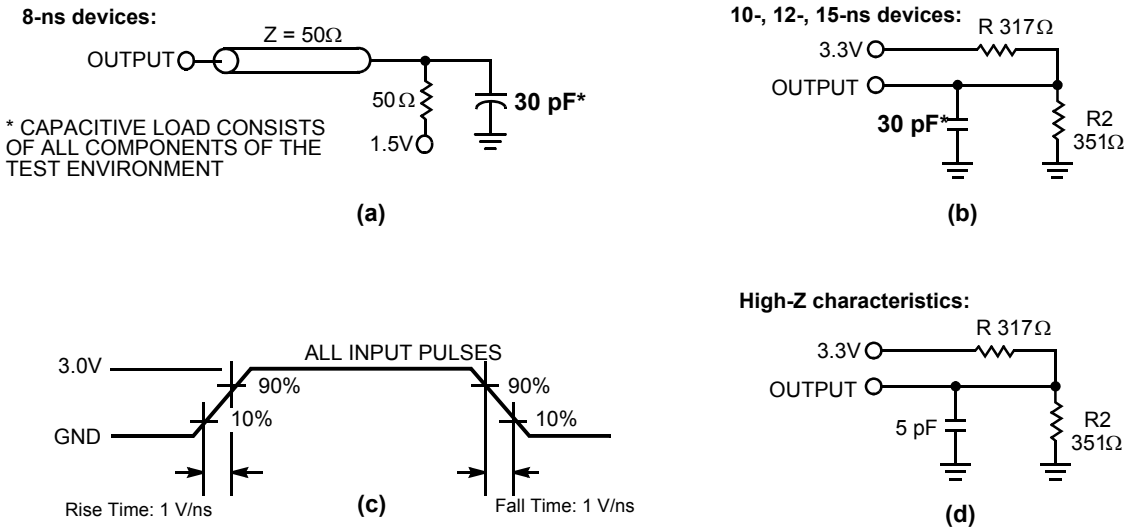
## Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

| Parameter | Description | Test Conditions | SOJ | TSOP II | FBGA | Unit |
|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51 | 65.06 | 76.92 | 95.32 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 34.21 | 15.86 | 10.68 | °C/W |

## AC Test Loads and Waveforms

**Figure 3. AC Test Loads and Waveforms** [4]




**Note**

4. AC characteristics (except High-Z) for all 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

## Switching Characteristics

Over the Operating Range [5]

| Parameter | Description | -8 | | -10 | | -12 | | -15 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | | | | | |
| $t_{power}$[6] | $V_{CC}$(Typical) to the First Access | 100 | | 100 | | 100 | | 100 | | µs |
| $t_{RC}$ | Read Cycle Time | 8 | | 10 | | 12 | | 15 | | ns |
| $t_{AA}$ | Address to Data Valid | | 8 | | 10 | | 12 | | 15 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 8 | | 10 | | 12 | | 15 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 5 | | 5 | | 6 | | 7 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z[7] | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[7, 8] | | 4 | | 5 | | 6 | | 7 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z[7] | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z[7, 8] | | 4 | | 5 | | 6 | | 7 | ns |
| $t_{PU}$[9] | $\overline{CE}$ LOW to Power Up | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$[9] | $\overline{CE}$ HIGH to Power Down | | 8 | | 10 | | 12 | | 15 | ns |
| $t_{DBE}$ | Byte Enable to Data Valid | | 5 | | 5 | | 6 | | 7 | ns |
| $t_{LZBE}$ | Byte Enable to Low Z | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZBE}$ | Byte Disable to High Z | | 4 | | 5 | | 6 | | 7 | ns |
| **Write Cycle**[10] | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 8 | | 10 | | 12 | | 15 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 7 | | 8 | | 9 | | 10 | | ns |
| $t_{AW}$ | Address Setup to Write End | 7 | | 8 | | 9 | | 10 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SA}$ | Address Setup to Write Start | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 6 | | 7 | | 8 | | 10 | | ns |
| $t_{SD}$ | Data Setup to Write End | 5 | | 5 | | 6 | | 8 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z[7] | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[7, 8] | | 4 | | 5 | | 6 | | 7 | ns |
| $t_{BW}$ | Byte Enable to End of Write | 6 | | 7 | | 8 | | 9 | | ns |

**Notes**

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V.
6. $t_{POWER}$ gives the minimum amount of time that the power supply is at typical $V_{CC}$ values until the first memory access is performed.
7. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
8. $t_{HZOE}$, $t_{HZBE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
9. This parameter is guaranteed by design and is not tested.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE}$/$\overline{BLE}$ is LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.

## Switching Waveforms

**Figure 4. Read Cycle No. 1 (Address Transition Controlled)[11, 12]**

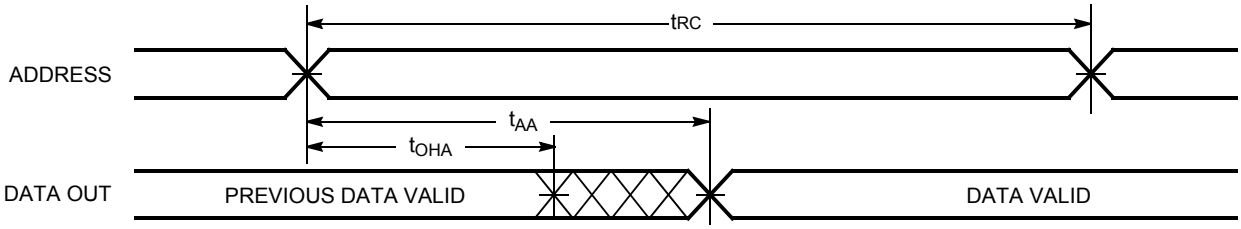
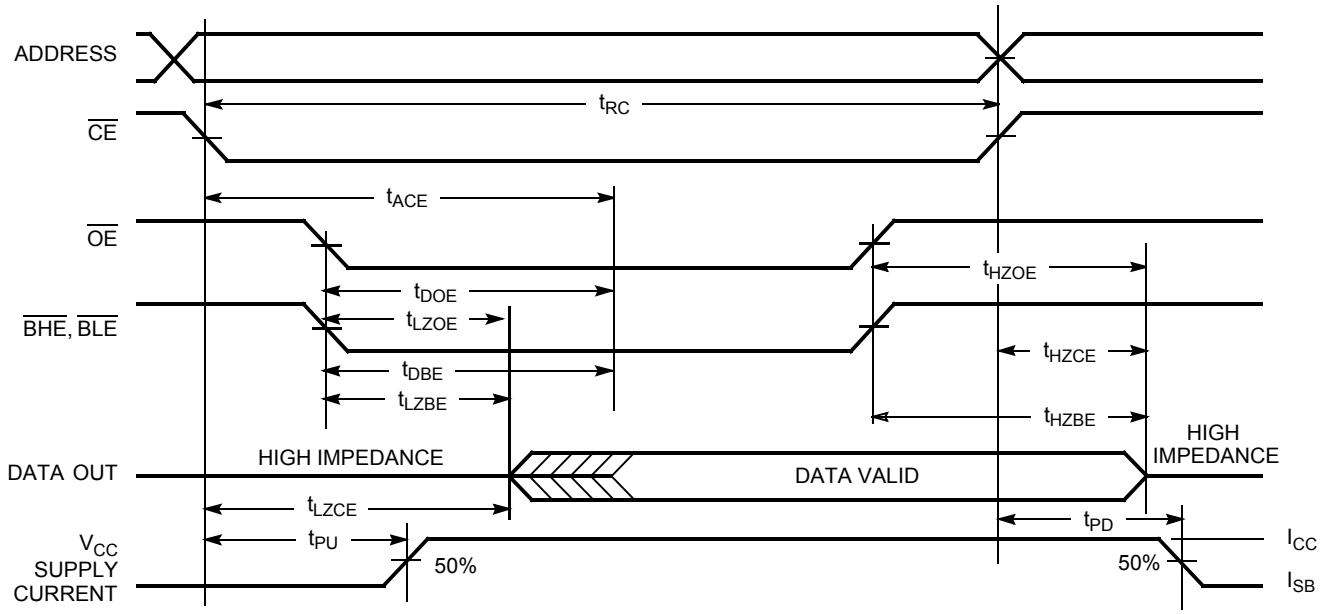



**Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]**




**Notes**
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = $V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled)[14, 15]**

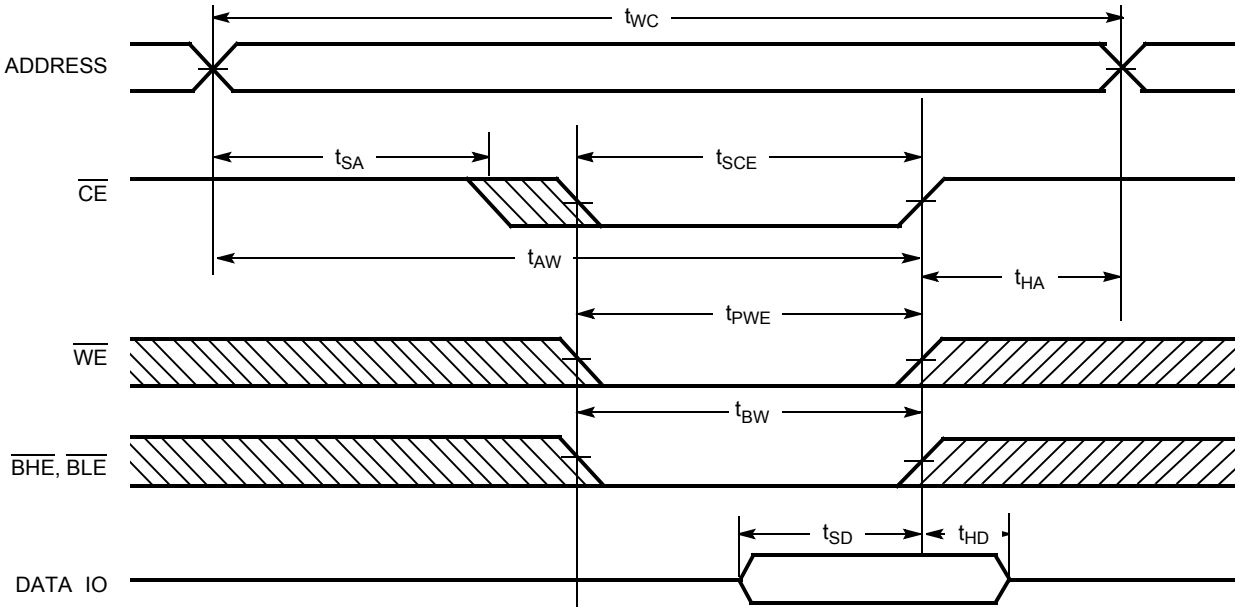
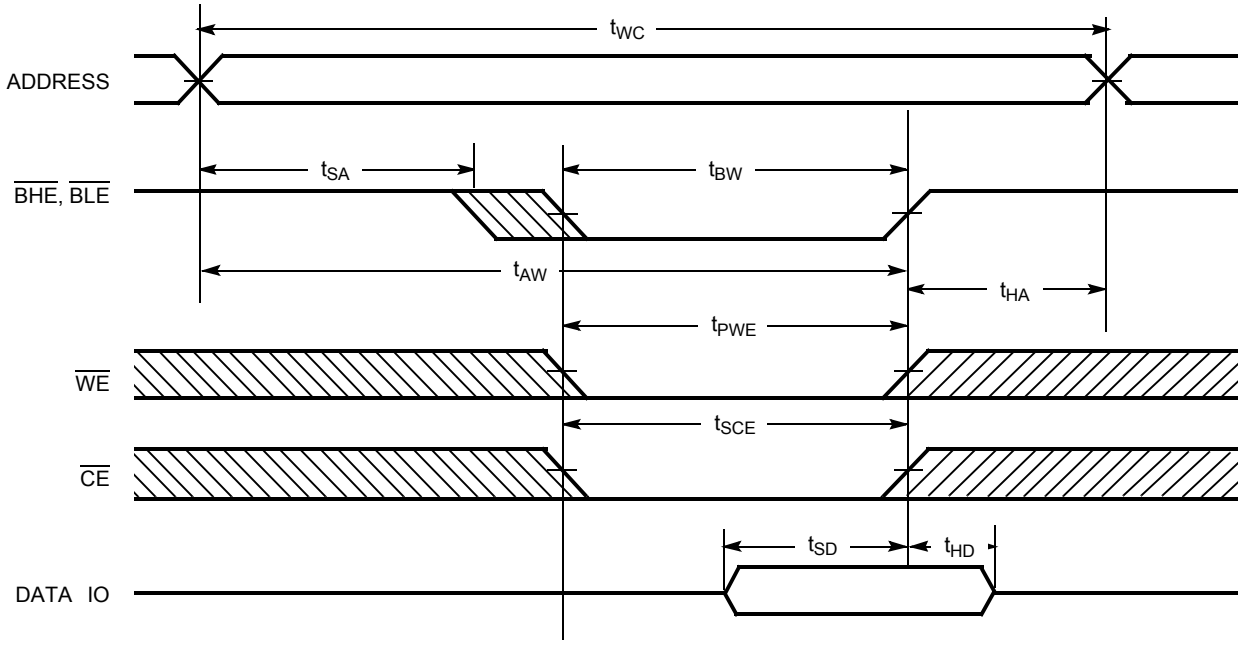


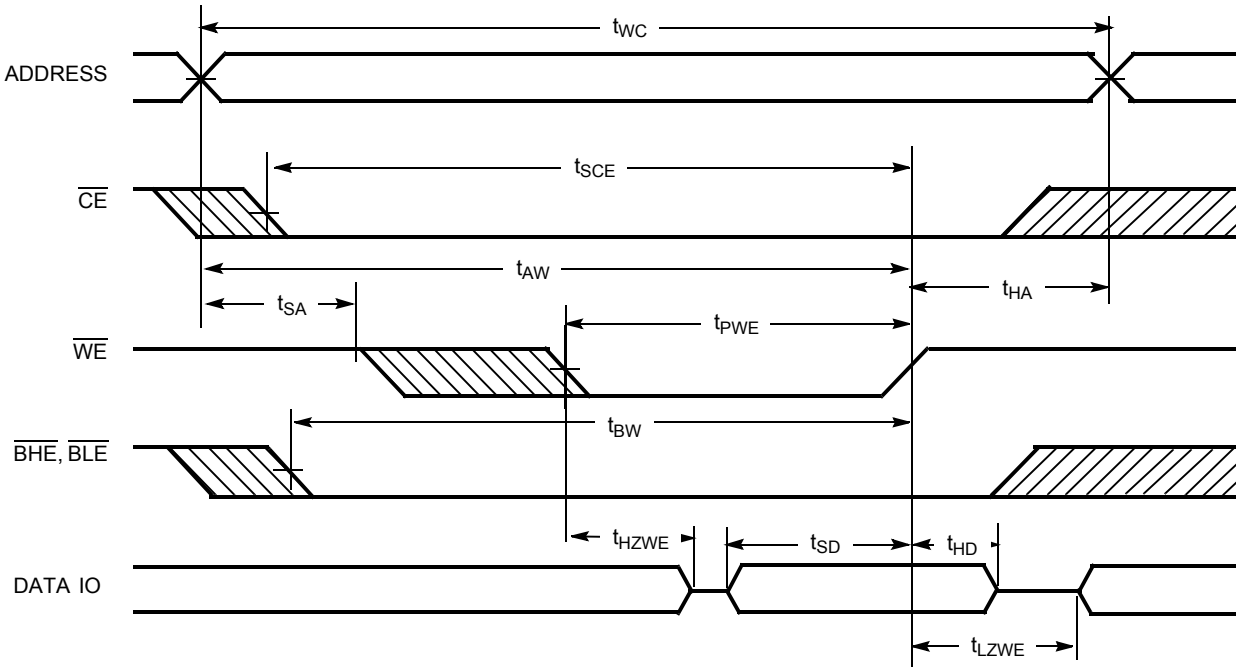

**Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)**




**Notes**
14. Data IO is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$= $V_{IH}$.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

## Switching Waveforms (continued)

**Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)**




## Truth Table

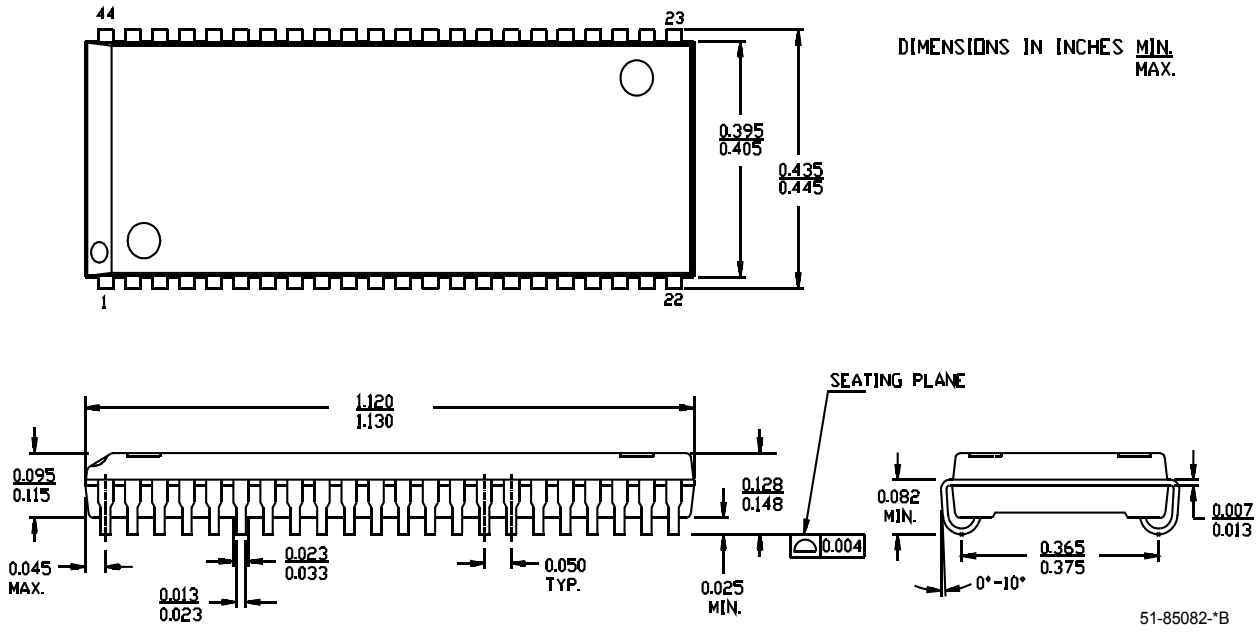
| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | $IO_1 – IO_8$ | $IO_9 – IO_{16}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | High Z | Power Down | Standby ($I_{SB}$) |
| L | L | H | L | L | Data Out | Data Out | Read – All Bits | Active ($I_{CC}$) |
| | | | L | H | Data Out | High Z | Read – Lower Bits Only | Active ($I_{CC}$) |
| | | | H | L | High Z | Data Out | Read – Upper Bits Only | Active ($I_{CC}$) |
| L | X | L | L | L | Data In | Data In | Write – All Bits | Active ($I_{CC}$) |
| | | | L | H | Data In | High Z | Write – Lower Bits Only | Active ($I_{CC}$) |
| | | | H | L | High Z | Data In | Write – Upper Bits Only | Active ($I_{CC}$) |
| L | H | H | X | X | High Z | High Z | Selected, Outputs Disabled | Active ($I_{CC}$) |
| L | X | X | H | H | High Z | High Z | Selected, Outputs Disabled | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 8 | CY7C1021CV33-8VXC | 51-85082 | 44-pin (400-Mil) Molded SOJ (Pb-free) | Commercial |
| | CY7C1021CV33-8ZXC | | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021CV33-8BAXC | 51-85096 | 48-ball FBGA (Pb-free) | |
| 10 | CY7C1021CV33-10VC | 51-85082 | 44-pin (400-Mil) Molded SOJ | Commercial |
| | CY7C1021CV33-10VXC | | 44-pin (400-Mil) Molded SOJ (Pb-free) | |
| | CY7C1021CV33-10ZXC | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021CV33-10ZI | 51-85087 | 44-pin TSOP Type II | Industrial |
| | CY7C1021CV33-10ZXI | | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021CV33-10BAXI | 51-85096 | 48-ball FBGA (Pb-free) | |
| 12 | CY7C1021CV33-12VC | 51-85082 | 44-pin (400-Mil) Molded SOJ | Commercial |
| | CY7C1021CV33-12VXC | | 44-pin (400-Mil) Molded SOJ (Pb-free) | |
| | CY7C1021CV33-12ZXC | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021CV33-12VI | 51-85082 | 44-pin (400-Mil) Molded SOJ | Industrial |
| | CY7C1021CV33-12VXI | | 44-pin (400-Mil) Molded SOJ (Pb-free) | |
| | CY7C1021CV33-12ZXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021CV33-12BAI | 51-85096 | 48-ball FBGA | |
| | CY7C1021CV33-12BAXI | | 48-ball FBGA (Pb-free) | |
| | CY7C1021CV33-12VE | 51-85082 | 44-pin (400-Mil) Molded SOJ | Automotive-E |
| | CY7C1021CV33-12VXE | | 44-pin (400-Mil) Molded SOJ (Pb-free) | |
| | CY7C1021CV33-12ZSE | 51-85087 | 44-pin TSOP Type II | |
| | CY7C1021CV33-12ZSXE | | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021CV33-12BAE | 51-85096 | 48-ball FBGA | |
| 15 | CY7C1021CV33-15VXC | 51-85082 | 44-pin (400-Mil) Molded SOJ (Pb-free) | Commercial |
| | CY7C1021CV33-15ZXC | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021CV33-15ZI | 51-85087 | 44-pin TSOP Type II | Industrial |
| | CY7C1021CV33-15ZXI | | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021CV33-15BAXI | 51-85096 | 48-ball FBGA (Pb-free) | |
| | CY7C1021CV33-15ZSXA | 51-85087 | 44-pin TSOP Type II (Pb-free) | Automotive-A |

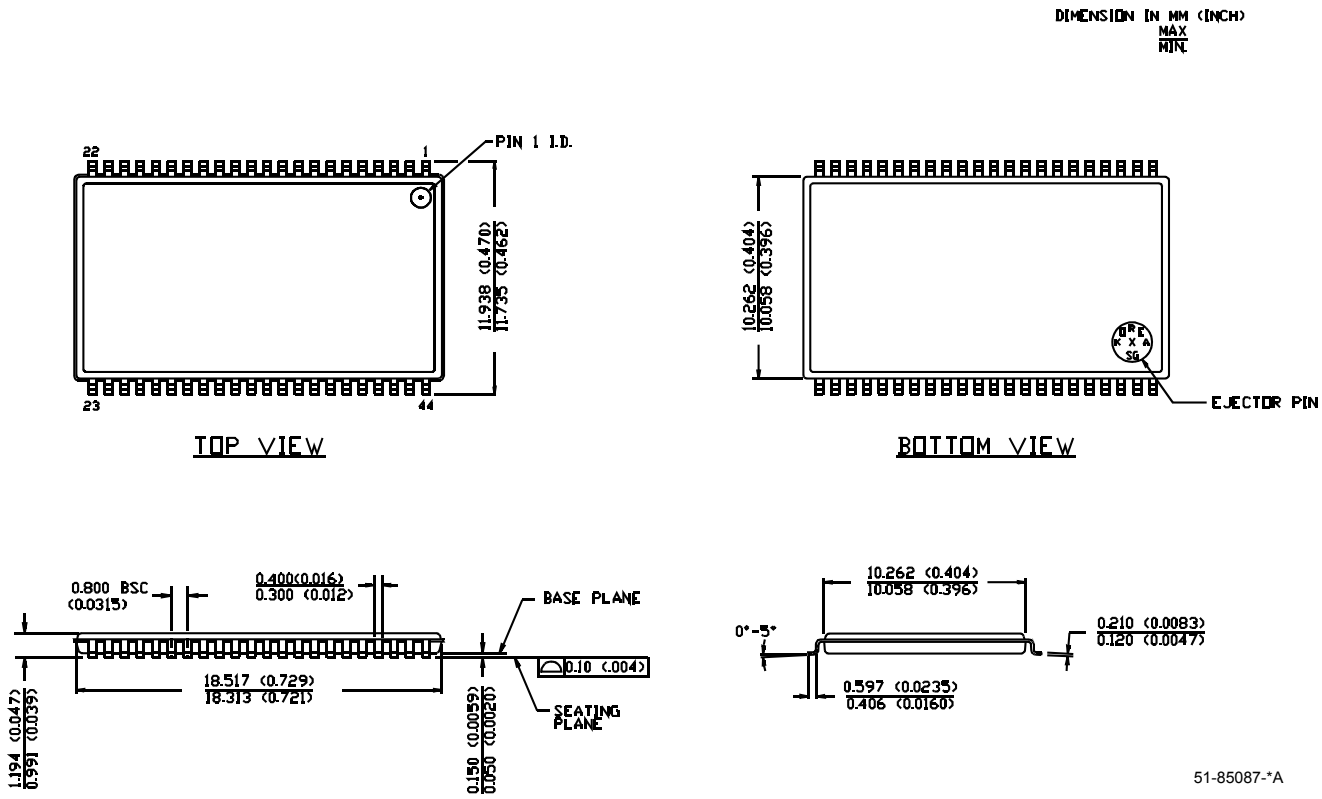
## Package Diagrams

**Figure 9. 44-Pin (400 Mil) Molded SOJ**



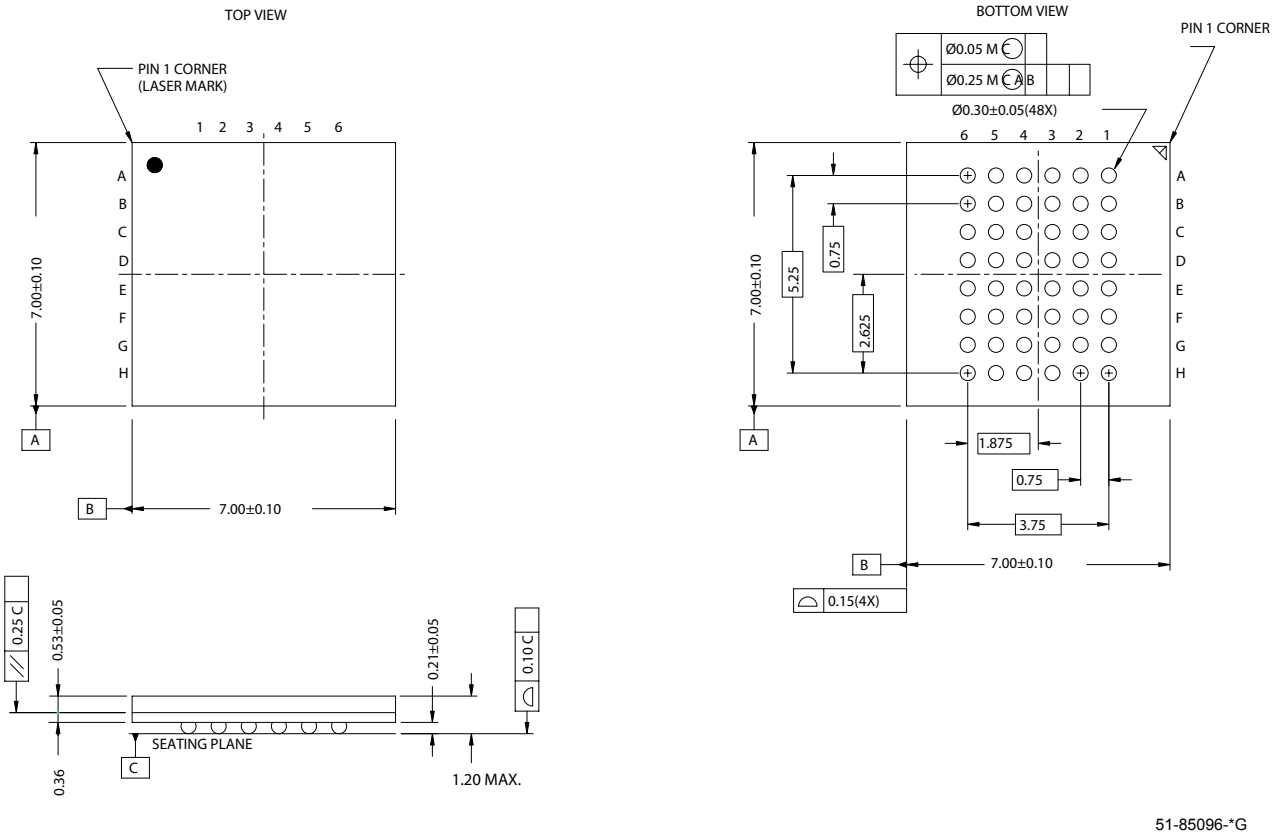
## Package Diagrams (continued)

**Figure 10. 44-Pin Thin Small Outline Package Type II**



## Package Diagrams (continued)

**Figure 11. 48-Ball FBGA (7 x 7 x 1.2 mm)**



## Document History Page

| Document Title: CY7C1021CV33, 1-Mbit (64K x 16) Static RAM<br>Document Number: 38-05132 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 109472 | 12/06/01 | HGK | New datasheet |
| *A | 115044 | 05/08/02 | HGK | Ram7 version C4K x 16 Async<br>Removed “Preliminary” |
| *B | 115808 | 06/25/02 | HGK | $I_{SB1}$ and $I_{CC}$ values changed |
| *C | 120413 | 10/31/02 | DFP | Updated BGA pin E4 to NC |
| *D | 238454 | See ECN | RKF | 1) Added Automotive Specifications to datasheet<br>2) Added Pb-free devices in the Ordering Information |
| *E | 334398 | See ECN | SYT | Added Pb-free on page 9 and 10 |
| *F | 493565 | See ECN | NXR | Added Automotive-A operating range<br>Corrected typo in the Pin Definition table<br>Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table<br>Removed $I_{OS}$ parameter from DC Electrical Characteristics table<br>Updated the ordering information table |
| *G | 563963 | See ECN | VKN | Added $t_{POWER}$ specification in the AC Switching Characteristics table<br>Added footnote 8 |
| *H | 1390863 | See ECN | VKN/AESA | Corrected TSOP II package outline |