LV5768V-A

Bi-CMOS IC

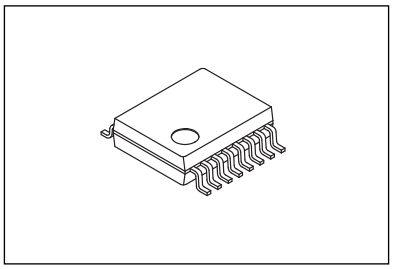
1-channel Step-down Switching Regulator

ON Semiconductor®

www.onsemi.com

Overview

The LV5768V-A is a 1-channel step-down switching regulator.



SSOP16(225mil)

Feature

- 1 channel step-down switching regulator controller.
- Frequency decrease function at pendent.
- Load-independent soft start circuit.
- ON/OFF function.
- Built-in pulse-by-pulse OCP circuit.
  It is detected by using ON resistance of an external MOS.
- Synchronous rectification
- Current mode control

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Supply voltage		V_{IN} max		45	V
Allowable pin voltage	V_{IN}, SW			45	V
	HDRV, CBOOT			52	V
	LDRV			6.0	V
	Between CBOOT to SW Between CBOOT to HDRV			6.0	V
	EN, ILIM			V_{IN}+0.3	V
	Between V_{IN} to ILIM			1.0	V
	V_{DD}			6.0	V
	SS, FB, COMP,RT			V_{DD}+0.3	V
Allowable Power dissipation		Pd max	Mounted on a specified board. *1	0.74	W
Operating temperature		Topr		-40 to +85	°C
Storage temperature		Tstg		-55 to +150	°C

*1 Specified board : 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{IN}		8.5 to 42	V
Error amplifier input voltage	V_{FB}		0 to 1.6	V
Oscillatory frequency	F_{OSC}		80 to 500	kHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Reference voltage block						
Internal reference voltage	Vref	Including offset of E/A	0.654	0.67	0.686	V
5V power supply	V_{DD}	I_{OUT} = 0 to 5mA	4.7	5.2	5.7	V
Triangular waveform oscillator block						
Oscillation frequency	F_{OSC}	RT=220kΩ	110	125	140	kHz
Frequency variation	$F_{OSC\ DV}$	V_{IN} = 8.5 to 42V		1		%
Oscillation frequency fold back detection voltage	$V_{OSC\ FB}$	FB voltage detection after SS ends		0.1		V
Oscillation frequency after fold back	$F_{OSC\ FB}$			$1/3F_{OSC}$		kHz
ON/OFF circuit block						
IC start-up voltage	V_{EN} on		2.5	3.0	3.5	V
IC off voltage	V_{EN} off		1.0	1.2	1.4	V
Soft start circuit block						
Soft start source current	I_{SS} SC	EN > 3.5V	4	5	6	μA
Soft start sink current	I_{SS} SK	EN < 1V, V_{DD} = 5V		2		mA
UVLO circuit block						
UVLO lock release voltage	V_{UVLO}			8		V
UVLO hysteresis	$V_{UVLO\ H}$			0.7		V
Error amplifier						
Input bias current	$I_{EA\ IN}$				100	nA
Error amplifier gain	G_{EA}		1000	1400	1800	μA/V
Sink output current	$I_{EA\ OSK}$	FB = 1.0V		-100		μA
Source output current	$I_{EA\ OSC}$	FB = 0V		100		μA
Current detection amplifier gain	GISNS			1.5		
over current limiter circuit block						
Reference current	$I_{LIM}1$		-10%	18.5	+10%	μA
Over current detection comparator offset voltage	$V_{LIM\ OFS}$		-5		+5	mV
Over current detection comparator common mode input range			V_{IN}-0.45		V_{IN}	V
PWM comparator						
Input threshold voltage (F_{OSC}=125kHz)	Vt max	Duty cycle = DMAX	0.9	1.0	1.1	V
	Vt0	Duty cycle = 0%	0.4	0.5	0.6	V
Maximum ON duty	DMAX		86	90	95	%
Output block						
Output stage ON resistance (the upper side)	R_{ONH}			5		Ω
Output stage ON resistance (the lower side)	R_{ONL}			5		Ω
Output stage ON current (the upper side)	I_{ONH}		240			mA
Output stage ON current (the lower side)	I_{ONL}		240			mA

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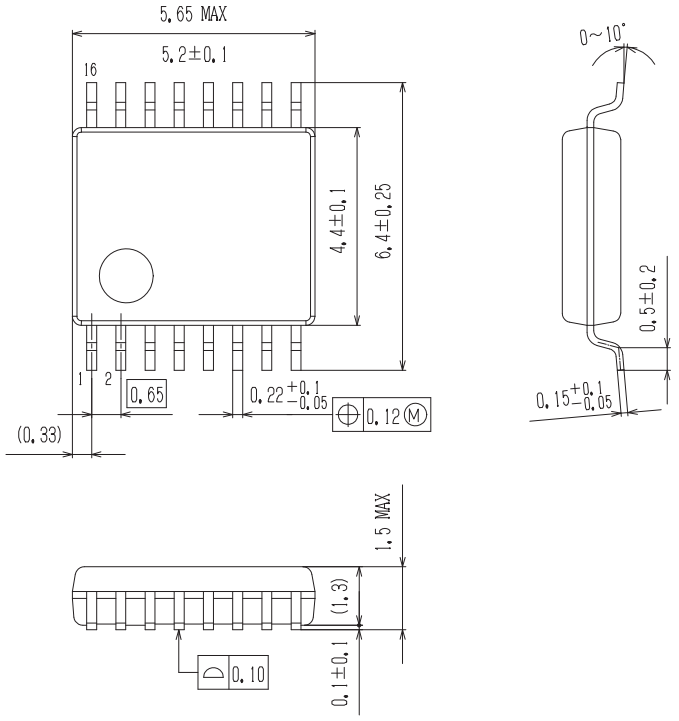
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
The whole device						
Standby current	I_{CCS}	EN < 1V			10	μA
Mean consumption current	I_{CCA}	EN > 3.5V		3		mA
Security function						
Protection function operating temperature at high temperature	TSD on	* Design certification		170		°C
Protection function hysteresis at high temperature	TSD hys	* Design certification		30		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

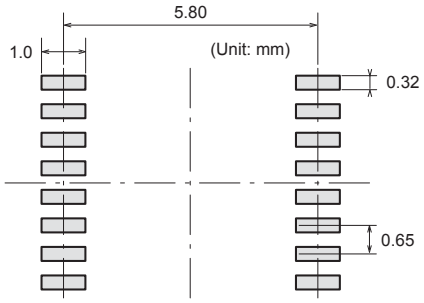
Package Dimensions

unit : mm

SSOP16 (225mil)
CASE 565AM
ISSUE A



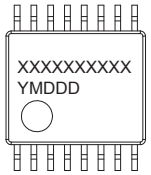
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

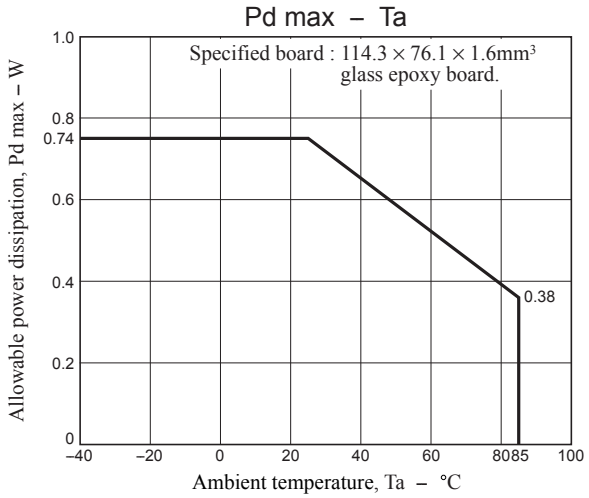
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

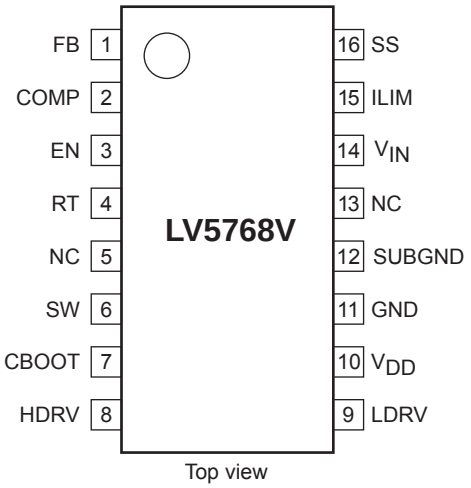


XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

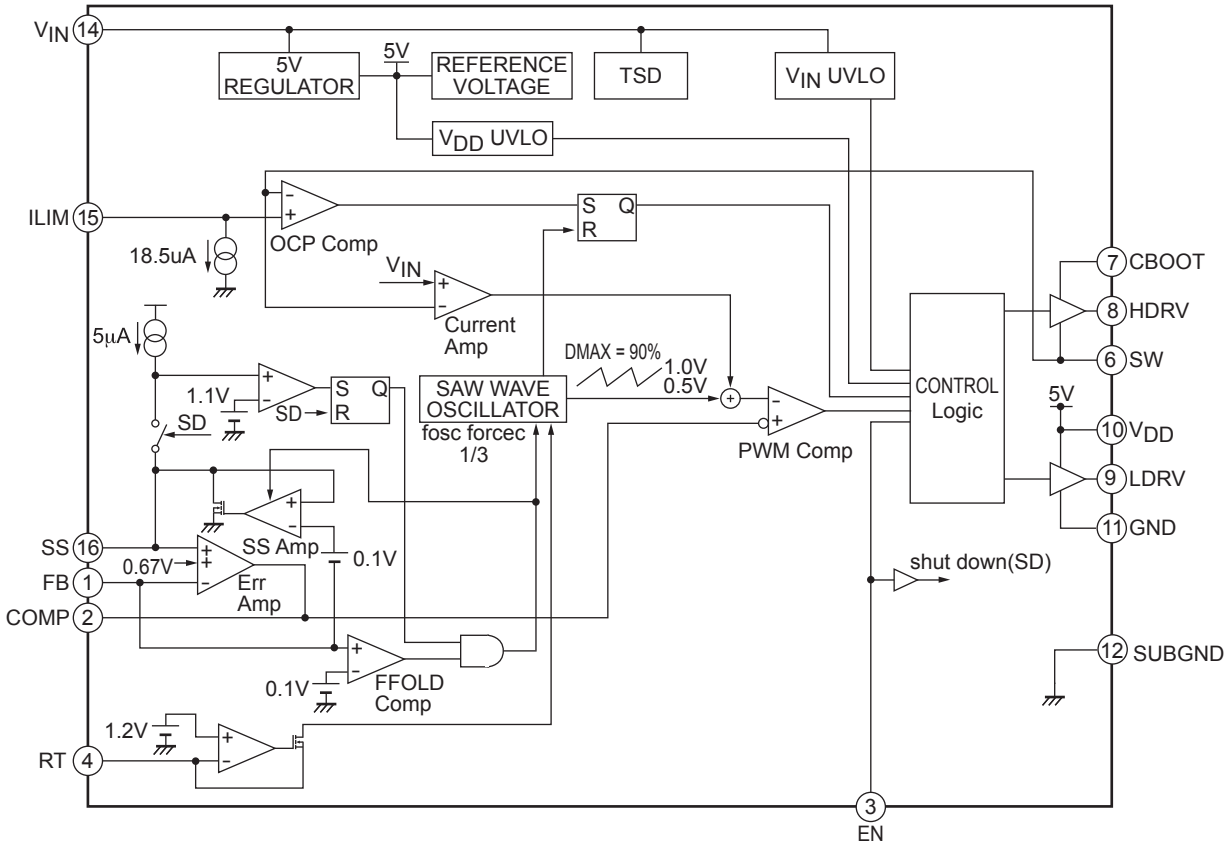
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.



Pin Assignment



Block Diagram



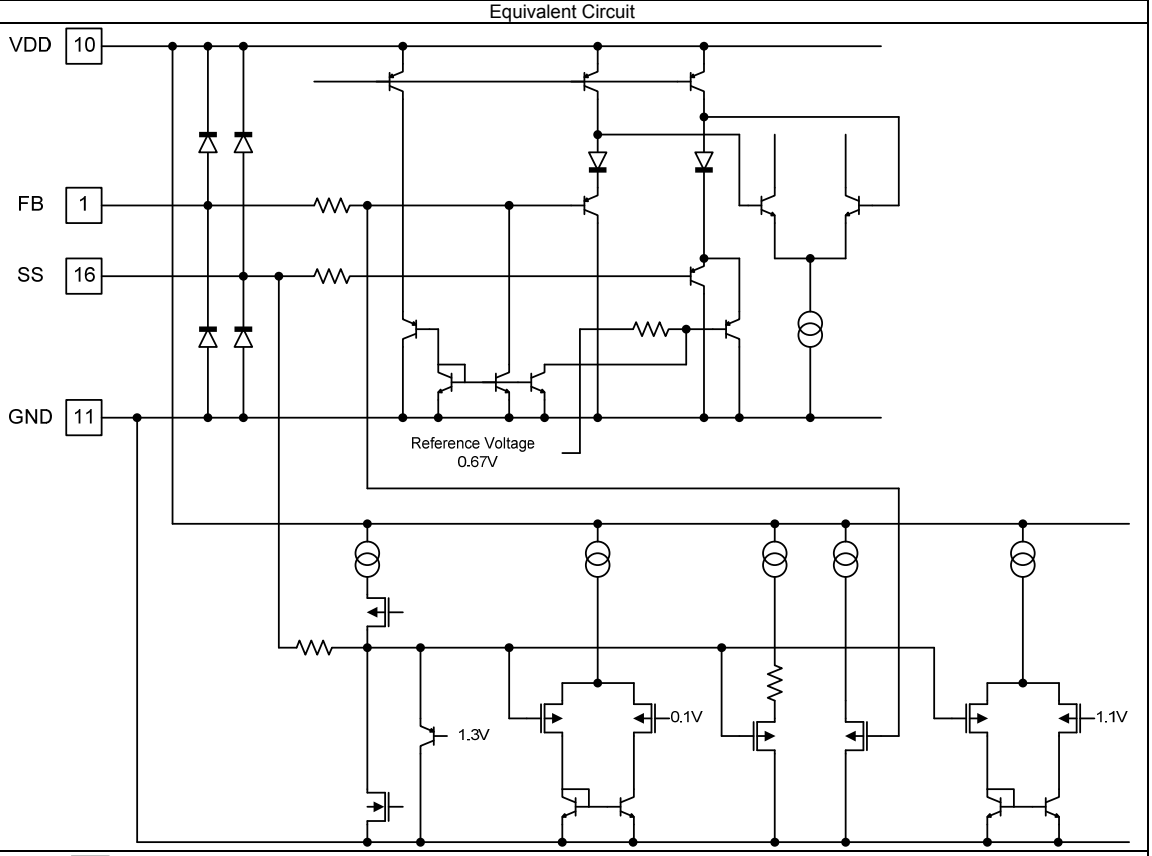
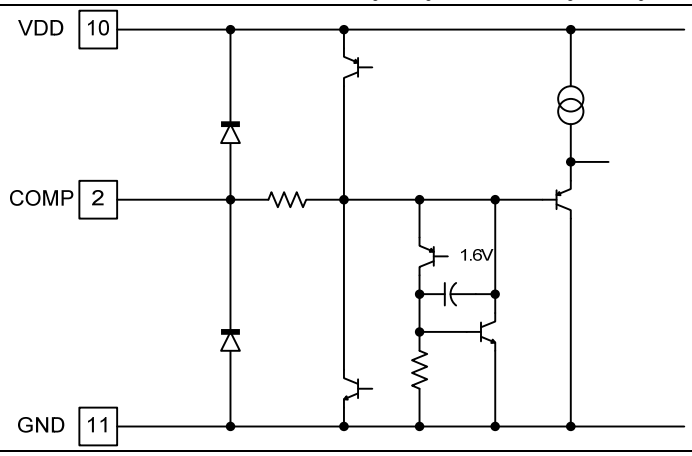
Pin Function

Pin No.	Pin name	Description
1	FB	Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.67V. The voltage in which the output voltage is divided by an external resistance is applied to this pin. Moreover, when this pin voltage becomes 0.1V or less after a soft start ends, the oscillatory frequency becomes 1/3.
2	COMP	Error amplifier output pin. Connect a phase compensation circuit between this pin and GND.
3	EN	ON/OFF pin.
4	RT	Oscillation frequency setting pin. Resistance is connected with this pin between GND.
5	N.C.	No connection *2
6	SW	Pin to connect with switching node. A source of external Upper NchMOSFET is connected with a drain of external lower NchMOSFET.
7	CBOOT	Bootstrap capacitor connection pin. This pin becomes a GATE drive power supply of an external NchMOSFET. Connect a bypath capacitor between CBOOT and SW.
8	HDRV	An external upper MOSFET gate drive pin.
9	LDRV	An external lower MOSFET gate drive pin.
10	V_{DD}	Power supply pin for an external the lower MOS-FET gate drive.
11	GND	Ground pin. Each reference voltage is based on the voltage of the ground pin.
12	SUBGND	It is connected with the GND pin of 11pin inside. *3
13	N.C.	No connection *2
14	V_{IN}	Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes 8V or more, the IC starts by UVLO function and the soft start function operates.
15	ILIM	Reference current pin for current detection. The sink current of about 18.5μA flows to this pin. When a resistance is connected between this pin and V_{IN} outside and the voltage applied to the SW pin is lower than the voltage of the terminal side of the resistance, the upper NchMOSFET is off by operating the current limiter comparator. This operation is reset with respect to each PWM pulse.
16	SS	Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the current of about 5μA. When this pin voltage becomes about 1.1V, the soft start period is expired. And the frequency fold back function becomes active.

*2 The problem does not occur even if connected to the GND.

*3 Short-circuit 11pin and 12pin.

I/O pin equivalent circuit chart

Pin No.	Equivalent Circuit
FB,SS	
COMP	

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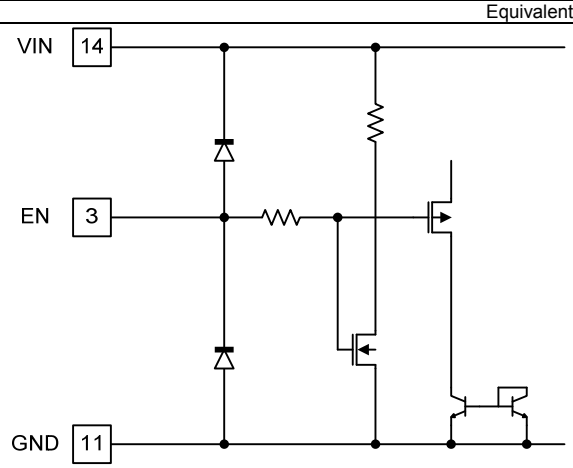
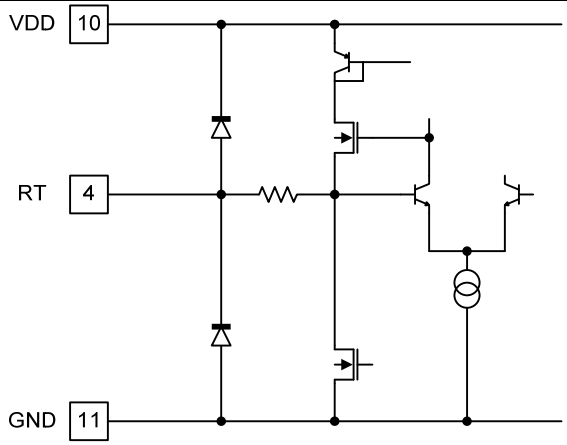
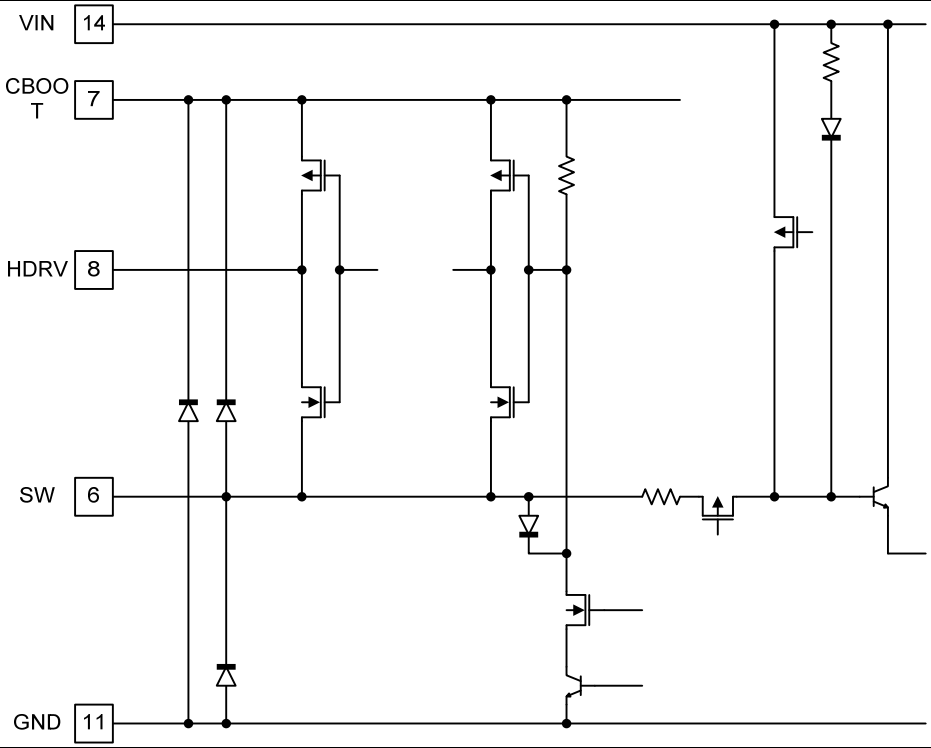
Pin No.	Equivalent Circuit
EN	
RT	
SW CBOOT HDRV	

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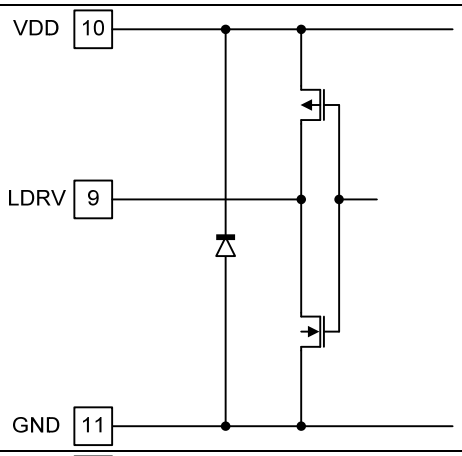
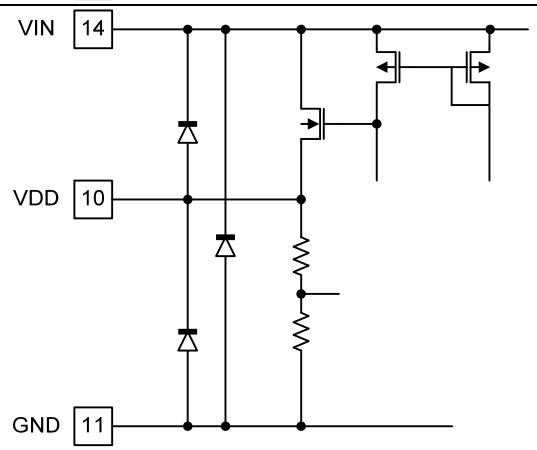
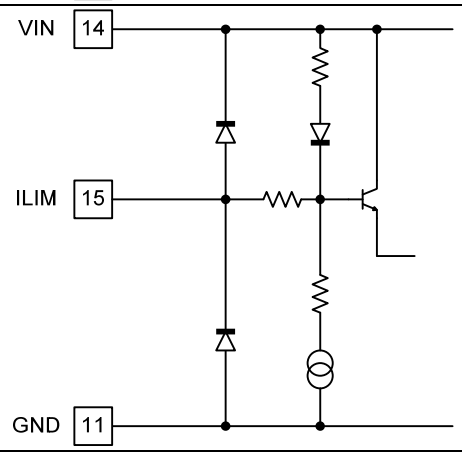
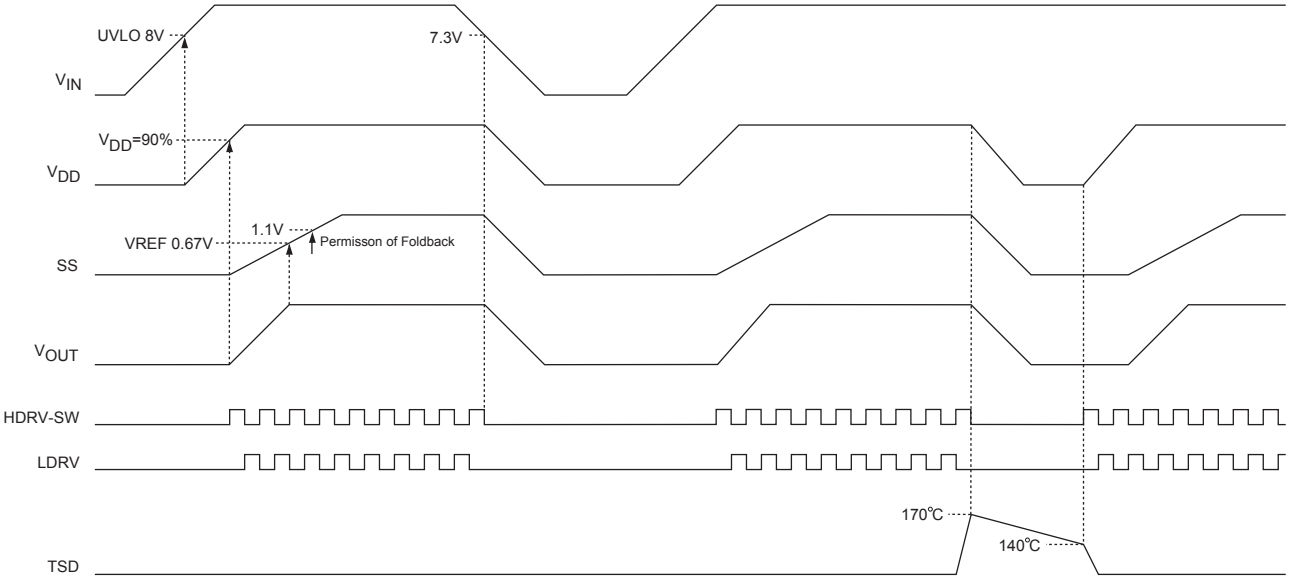
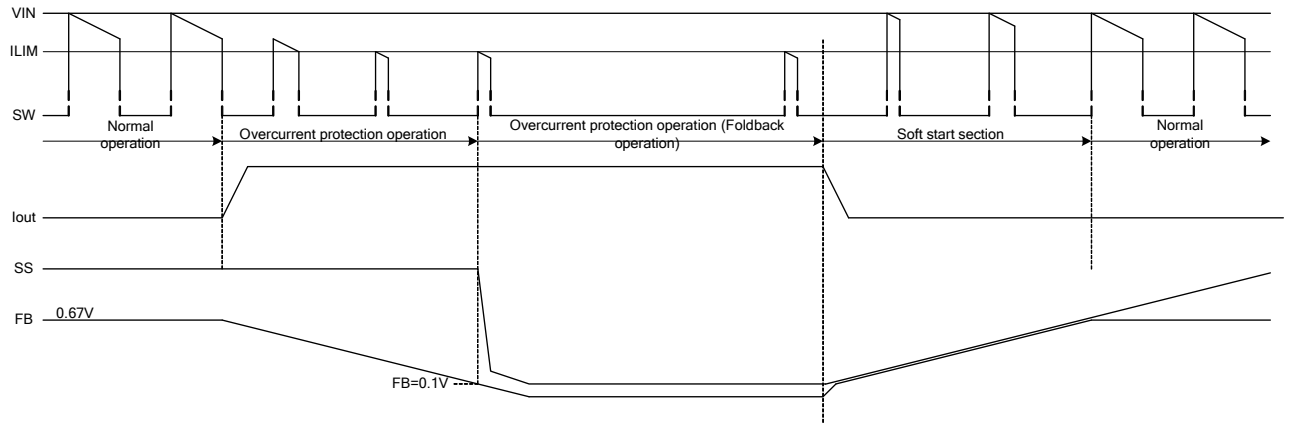
Pin No.	Equivalent Circuit
LDRV	
VDD	
ILIM	

Boot sequence, UVLO, and TSD operation

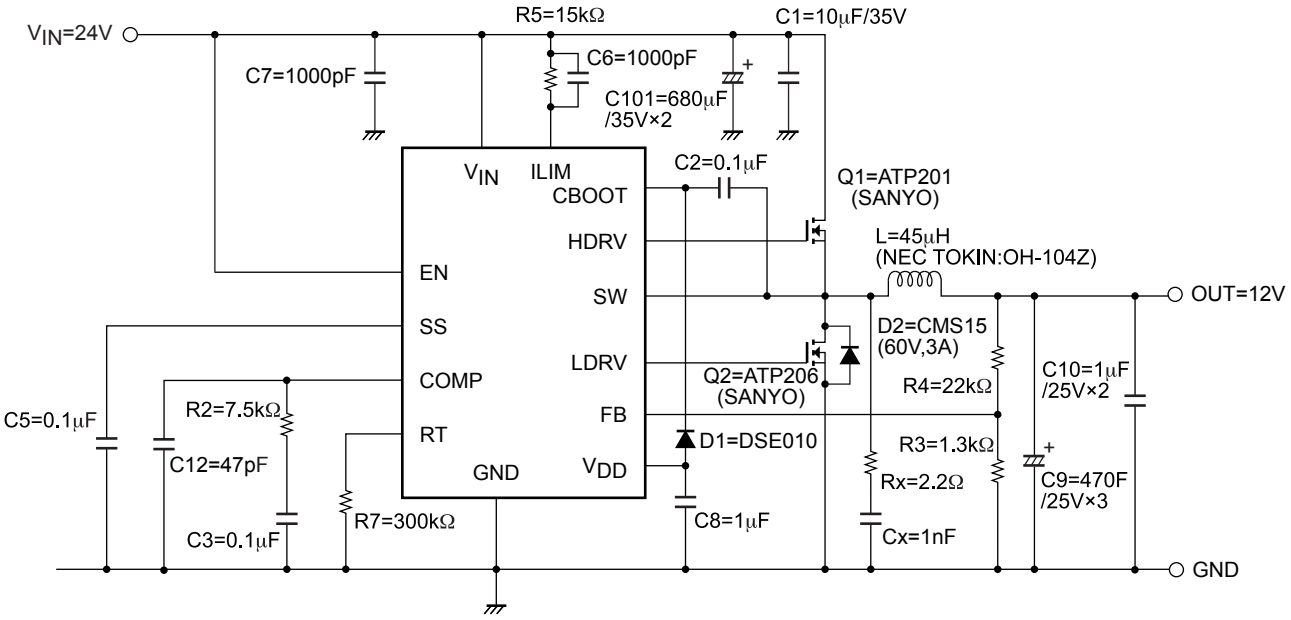


Sequence of overcurrent protection



Sample Application Circuit

V_{IN}=24V, V_{OUT}=12V, I_{OUT}=7A, Fosc=100kHz



• Part selection and set

1) Output voltage set

Output voltage (V_{OUT}) is shown the equation (1).

$$V_{OUT} = (1 + \frac{R4}{R3}) \times VREF = (1 + \frac{22k\Omega}{1.3k\Omega}) \times 0.67\ (typ) \quad [V] \qquad (1)$$

Ex) To set output voltage of 12V, set resistors as follows: R3=1.3kΩ and R4=22kΩ.

2) Soft start set

Soft start capacitor (C5) is obtained by the equation (2).

$$C5 = \frac{I_{SS} \times T_{SS}}{V_{REF}} = \frac{5\mu \times T_{SS}}{0.67V} \quad [\mu F] \qquad (2)$$

I_{SS}: Charge current value, T_{SS}: soft start time

Ex) To set soft start time of 15ms (approx.), set C5=0.1μF.

3) Overcurrent protector set

Overcurrent limit setting resistor (R5) is obtained by the equation (3).

$$R5 = \frac{Rdson \times I_{L\ max}}{I_{lim}} = \frac{Rdson \times IL\ max}{18.5\mu} \quad [\Omega] \qquad (3)$$

I_{lim}: ILIM current value,

ILmax: the maximum value of coil current,

Rdson: Ron between drain and source of Q1 (upper Nch MOS FET).

Ron of ATP201 ≈ 23mΩ (when VGS=4.5V at 25°C)

Ex) To set current limit operation point to 11.3A (load current) where coil peak current value is 12A (approx.), set R5 = 15kΩ. Set an optimum resistor taking variation of ON resistance into consideration due to temperature change and make sure to confirm it with the user's specific board. For C6, connect a capacitor of 1000pF to filter unwanted noise for the proper operation of current limiting.

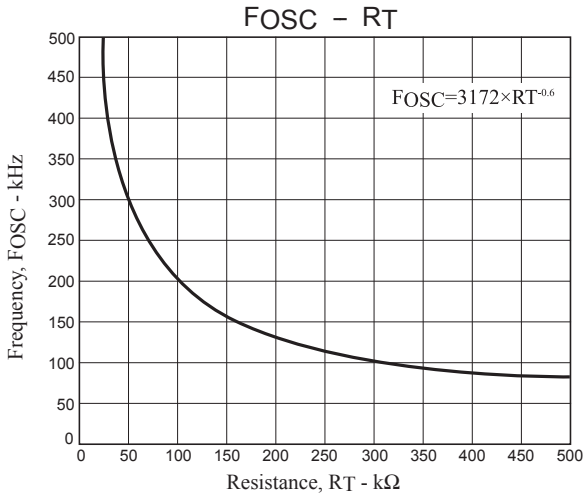
ON resistance of FET

* Rdson of FET has its own temperature coefficient and the resistor becomes higher in proportion to the temperature.
* To set Rdson value within the range of operating temperature, it is advisable that the user confirm the data sheet by the FET supplier.

4) How to set oscillation frequency

Oscillation frequency Fosc is adjustable by RT resistor as shown in the correlation chart as follows:

SW frequency setting range: 80kHz to 500kHz



5) Boot strap capacitor set

For boot strap capacitor C2, use capacitor 100 times larger than Ciss of power MOSFET.

6) Phase compensation set

Since LV5768V adopts current mode control, low ESR capacitor and solid polymer capacitor such as OS capacitor can be used as output capacitor with simple phase compensation.

***Frequency characteristics**

Frequency characteristics of LV5768V consist of the following transfer functions.

(1) Output resistor divider ; H_R
(2) Voltage gain of error amplifier ; G_{VEA}
Current gain (Transconductance) ; G_{MEA}
(3) Impedance of external phase compensation part ; Z_C
(4) Current sense loop gain ; G_{CS}
(5) Output smoothing impedance ; Z_O

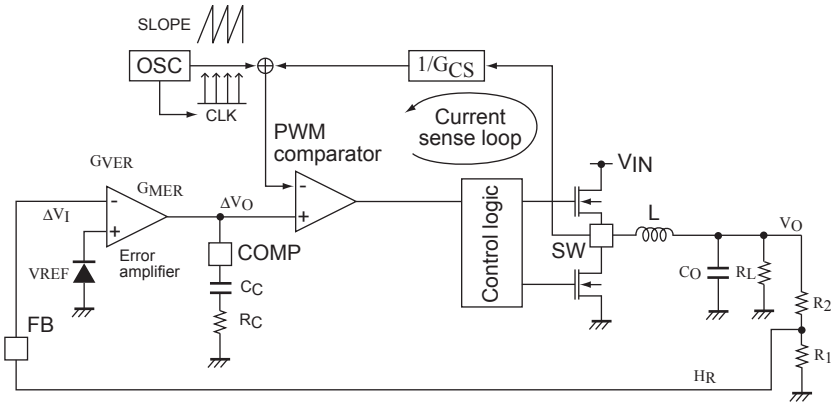


Fig. Current control loop of LV5768V

Closed loop gain is obtained by the equation (4)

$$G = H_R \times G_{MEA} \times Z_C \times G_{CS} \times Z_O$$

$$R5 = \frac{V_{REF}}{V_O} \times G_{MEA} \times \left(R_C + \frac{1}{SC_C}\right) \times G_{CS} \times \frac{R_L}{1 + SC_OR_L} \quad (4)$$

From the equation (4), the frequency characteristics of closed loop gain is given by pole fp1 which consists of output capacitor Co and output load resistor RL, zero point fz which is given by external resistor Rc and capacitor Cc of phase compensation pin COMP and pole fp2 which is given by output impedance of error amplifier Z_{EA} and external phase compensation capacitor Cc. fp1, fz, fp2 are given by the equation (5), (6) and (7).

$$fp1 = \frac{1}{2\pi C_OR_L} \quad (5), \quad fz = \frac{1}{2\pi C_CR_C} \quad (6), \quad fp2 = \frac{1}{2\pi \times Z_{EA} \times C_C} \quad (7)$$

*****Calculation of the phase compensation by external part R_C and C_C

In general, the frequency where closed loop gain becomes 1 (zero cross frequency fzc) should be 1/10 of the switching frequency (or 1/5 at the highest) to stabilize the operation of switching regulator.

Ex) When switching frequency of LV5768V is 100kHz:

$$fzc = \frac{100kHz}{10} \approx 10kHz \quad (8)$$

Since the closed loop gain becomes 1 with this frequency, the equation (7) = 1

$$\frac{V_{REF}}{V_O} \times G_{MEA} \times \left(R_C + \frac{1}{SC_C}\right) \times G_{CS} \times \frac{R_L}{1+SC_OR_L} = 1 \quad (9)$$

In reality for zero cross frequency, since capacity element $\frac{1}{SC_C}$ of phase compensation becomes lower enough than the resistance element R_C: $R_C \gg \frac{1}{SC_C}$ (10)

The equation (9) becomes $$\frac{V_{REF}}{V_O} \times G_{MEA} \times R_C \times G_{CS} \times \frac{R_L}{1+2\pi \times f_{ZC} \times C_O \times R_L} = 1 \quad (11)$$

From the equation, phase compensation external resistor R_C is obtained by the following formula. However, G_{CS}=0.67/Rdson=29A/V, G_{MEA}=1400µA/V.
Given that output is 12V and load resistor is 1.7Ω (7A load):

$$\therefore R_C = \frac{V_O}{V_{REF}} \times \frac{1}{G_{MEA}} \times \frac{1}{G_{CS}} \times \frac{1+2\pi \times f_{ZC} \times C_O \times R_L}{R_L} \quad (12)$$

$$= \frac{12}{0.67} \times \frac{1}{1400\mu A/V} \times \frac{1}{29A/V} \times \frac{1+2\pi \times 10k \times 1410\mu \times 1.7}{1.7}$$

$$\approx 39k\Omega \quad (13)$$

This is the external resistor value R_C obtained from this calculation (the calculation reveals that the last block where load resistor R_L is inserted is 1 « $2\pi \times f_{ZC} \times C_O \times R_L$. Therefore, there is no dependence on R_L.).
When point zero f_Z (6) and pole fp1 (5) are the same values, they cancel out each other. Hence, there is only one pole frequency for the phase characteristics of closed loop gain. In other words, you can obtain characteristics in which waveform is stable because the gain frequency lowers at -20dB/DEC and phase only rotates by -90 degree.

Since (6) = (5) $f_Z = fp1$ (14)

$$\frac{1}{2\pi C_C R_C} = \frac{1}{2\pi C_O R_L}$$

$$\therefore C_C = \frac{R_L \times C_O}{R_C} = \frac{1.7 \times 1410\mu}{39k} = 0.062\mu F$$

The external resistor value R_C and capacitor value C_C between phase compensator pin COMP and GND is obtained as such using ideal equations. In reality, stable phase margin should be defined based on testing under the entire temperature, load and input voltage range. On the other hand, such ideal value is used as starting point for the assessment. In the deliverable evaluation board, the above values are used as defaults. C_C and R_C are defined according to conditions of transient response too. If the influence of noise is significant, it is advisable to increase the capacitance of C_C.

7) Input capacitor selection

When switching of the IC occurs, ripple current flows into the input capacitor of DC-DC converter. Like input current, the more the output current flows, the more the ripple current into input capacitor flows. Also, the lower the input voltage is, the more the duty expands. As a result, the ripple current flows more. Allow higher ripple current than the result of the equation. The input capacitor should be connected adjacent to the power IC and minimize the inductance from the pattern layout. Root mean squared value is obtained by the equation (15).

$$Irip\_in = \sqrt{D(1-D)} \times I_{OUT} \quad [Arms] \quad (15)$$

D represents duty cycle defined by V_{OUT}/V_{IN}.

8) Output capacitor selection

If ceramic capacitor is used to output, output ripple voltage is obtained as follows since ESR of capacitance is small.

$$Vrip = \frac{V_{OUT}}{8 \times L \times C_O \times f_{OSC}^2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad [V] \quad (16)$$

Also if electrolytic capacitor is used to output, output ripple voltage is affected by ESR since ESR of capacitance is large. In this case, output ripple voltage is obtained by the following equation.

$$Vrip = \frac{V_{IN} - V_{OUT}}{f_{OSC} \times V_{IN}} \times \frac{V_{OUT} \times R_{ESR}}{L} \quad [V] \quad (17)$$

Since the allowable ripple current of electrolytic capacitor is lower compared to that of ceramic capacitor, the allowable ripple current value must not be exceeded. Root mean squared value is obtained by the following equation.

$$Irip\_out = \frac{1}{\sqrt[2]{3}} \times \frac{V_{OUT}\,(V_{IN} - V_{OUT})}{L \times f_{OSC} \times V_{IN}} \quad [Arms] \tag{18}$$

It is advisable to use ceramic capacitor in combination with electrolytic capacitor to reject high frequency noise. The electrolytic capacitor can be low ESR aluminum electrolytic capacitor or polymer aluminum electrolytic capacitor.

9) Inductor selection

L1: Caution is required due to the heat generation of choke coil caused by overload and load short. The inductance value is determined by output ripple voltage (Vrip) and the impedance of output capacitor for switching frequency. The minimum inductance is obtained by the equation (19).

$$L\ min = \frac{V_{IN} - V_{OUT}}{f_{OSC} \times V_{IN}} \times \frac{V_{OUT} \times R_{ESR}}{Vrip} \quad [\mu H] \tag{19}$$

In the above equation, ESR is used in place of the impedance of output capacitor. The reason is, the impedance of output capacitor for switching frequency is close to R_{ESR} in many cases. However with ceramic capacitor, real impedance is used instead of R_{ESR}.

Ex)V_{IN}(max)=24V, V_{OUT}=12V, Vrip=20mV, R_{ESR}=9mΩ, f_{OSC}=100kHz

$$L\ min = \frac{24V - 12V}{100k \times 24V} \times \frac{12V \times 9m}{20mV} \tag{20}$$

$$\approx 27\ [\mu H]$$

In the actual part selection, ripple voltage is defined first, then capacitor and inductor are selected. Take the maximum value and minimum value of input voltage, output voltage and load variation into consideration. Also, the ripple current of inductor is used as basis for output inductor selection in many cases. Ripple current is obtained by the equation (21).

$$Irip = \frac{V_{IN} - V_{OUT}}{f_{OSC} \times L} \times D \quad [A] \tag{21}$$

D represents duty cycle defined by V_{OUT}/V_{IN}.

The important term is the ripple current represented as $Irip/I_{OUT}$. As long as the ripple element is less than 50%, it should not be a problem. If the ripple element is higher, inductor loss becomes significant.

Ex)V_{IN}=24V, V_{OUT}=12V, f_{OSC}=100kHz, L=45μH

$$Irip = \frac{24V - 12V}{100k \times 45\mu} \times 0.5 \tag{22}$$

$$= 1.3\ [A]$$

10) Power consumption of high side MOSFET

The power consumption in the external high side MOSFET is represented by conduction loss and switching loss. The conduction loss of MOSFET is obtained by the following equation (23).

$$Psat = I_O^2 \times R_{DS(ON)} \times D \quad [W] \tag{23}$$

Since $R_{DS(ON)}$ is affected by temperature, it is advisable to confirm the actual FET temperature and data sheet.

The switching loss of high side MOSFET is obtained by the following equation (24).

$$Psw = V_{IN} \times I_O \times t_{SW} \times f_{SW} \quad [W] \tag{24}$$

I_O: DC output current
t_{SW}: Rise time of switching waveform
f_{SW}: Switching frequency

The junction temperature of high side MOSFET is obtained by the following equation (25).

$$Tj = Ta + (Psat + Psw) \times \theta ja \quad [W] \tag{25}$$

θja: heat resistor between junction and ambient.
Tj should not exceed the Tjmax as stated in the data sheet.

11) Power consumption of low side MOSFET

The power consumption in low side MOSFET consists of conduction loss from $R_{DS\ (ON)}$ as well as from body diode and reverse recovery loss. The conduction loss due to $R_{DS\ (ON)}$ is obtainable by the equation (23) which is represented in the equation (26).

$$Psat = I_O^2 \times R_{DS(ON)} \times (1\text{-}D) \quad [W] \tag{26}$$

The conduction loss from body diode occurs when the body diode is conducted forwardly between high side off and low side off zone, which is represented in the equation (27).

$$Pdf = 2 \times I_O \times Vf \times tdelay \times f_{SW} \quad [W] \tag{27}$$

Vf: Forward voltage of body diode
tdelay: Delay time immediately before surge of SW node

The total power consumption of low side MOSFET is obtained by the equation (28).

$$Pls = Psat + Pdf \quad [W] \tag{28}$$

12) Power consumption of LV5768V

The total power consumption of LV5768V is represented in the equation (29) given that the same MOSFET is selected for high side and low side.

$$Pd\_ic = (2 \times Qg \times f_{SW} + I_{CC}A) \times V_{IN} \quad [W] \tag{29}$$

$I_{CC}A$: IC consumption current when switching is stopped.

- Caution for pattern layout

C1: input capacitor

When the IC performs switching, a ripple current flows into the input capacitor of DC-DC converter. The capacitor of input should be connected adjacent to the power IC and minimize the inductance from pattern layout. C1 should be connected adjacently to V_{IN} pin of the IC and Q1 (high side FET- drain). If implementation to IC side is not feasible, insert adjacently to Q1.

C7 (bypass capacitor connected to V_{IN} pin of the IC) should be connected adjacently to V_{IN} pin and GND pin. In rare cases, intensive ringing may occur in the V_{IN} pin by connecting bypass capacitor. The recommendation value is 1000pF.

Q1, Q2 (D1): external FET

Both high and low sides are driven by Nch-MOSFET. In Q1, a transition of SW node takes place between V_{IN} and GND by turn on and off, where high frequency noise occurs. The noise affects the surrounding pattern layouts and parts. The high/ low side gate and SW node should be laid out as fat and short as possible and connect to HDRV, LDRV and SW pins of the IC. HDRV, LDRV and SW pins should be shielded with GND to prevent influence from noise.

When high side FET is turned on, ripple current path is as follows: V_{IN} + (C1) --> Q1--> inductor (L) --> C9 --> GND. When low side FET is turned on, current path is as follows: Q2(D1) --> inductor (L) --> C9 --> GND. By minimizing the area of current path and keeping the pattern layout fat and short, noise is eliminated and error operation is prevented. Hence, Q1, Q2, D1, C1 and C9 should be implemented nearby.

R5,C6: ILIM (overcurrent limiter set pin)

ILIM pin detects overcurrent which is used as set point where current limit comparator in the IC starts operation. The overcurrent limiter is adjustable by the resistor between I_{LIM} pin and V_{IN} pin. When the voltage of SW pin becomes lower than that of I_{LIM} pin, current limit comparator functions and turns off the high side MOSFET. This operation is reset at every PWM pulse.

To filter unwanted noise, C6 should be connected in parallel to the set resistor (the recommendation is 1000pF). R5 and C6 should be implemented adjacently to the V_{IN} side of the IC. If they are apart from the V_{IN} side, detection precision for overcurrent point may be deteriorated.

Small signal blocks: part for FB, COMP, EN, CBOOT, V_{DD} and SS pins.

The parts should be implemented adjacently to the IC and be connected as short as possible. Also the GND of the parts should have common GND pattern as the IC. FB pattern layout should not be under nor nearby the inductor or SW node. This must be complied to avoid error operation.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5768V-A-TLM-E	SSOP16 (225mil) (Pb-Free)	2000 / Tape & Reel
LV5768V-A-MPB-E	SSOP16 (225mil) (Pb-Free)	90 / Fan-Fold