Quad Power Supply Sequencer

FEATURES

- **Fully Sequence and Monitor Four Supplies**
  - **Six with Minimal External Circuitry**
- **Cascadable for Additional Supplies**
- **Power Off in Reverse Order or Simultaneously**
- **Charge Pump Drives External MOSFETs**
- **Drives Power Supply Shutdown Pins with No External Pull-Up Resistors**
- 10µA Output Current Allows Soft-Starting of Supplies
- Done Indicator for Both Power On and Power Off
- Adjustable Time Delay Between Power Supplies
- Power Good Timer
- Power Supply Voltage Monitoring and Power Sequence Error Detection and Reporting
- Available in a 16-Lead Narrow SSOP Package

APPLICATIONS

- Sequenced Power Supplies for ASICs with Multiple I/O and Core Voltages
- Latch-Up Prevention in Systems with Multiple Power Supplies

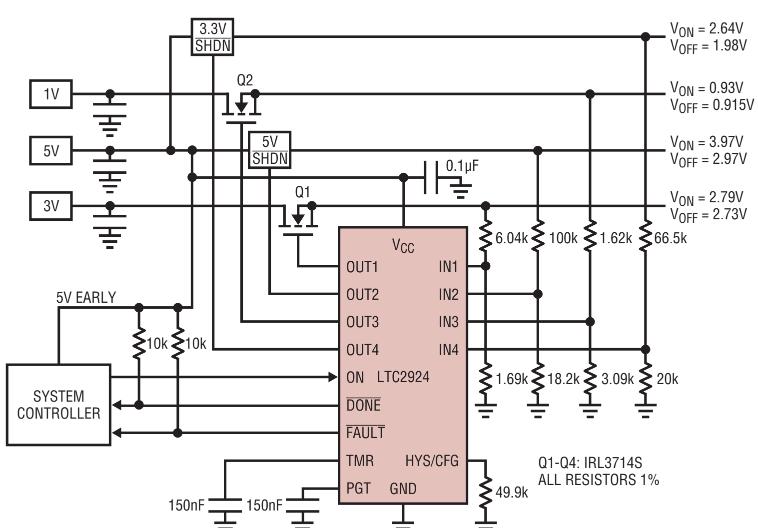
DESCRIPTION

The LTC®2924 is a power supply sequencer designed for use with external N-channel MOSFETs or power supplies with shutdown pins. Four power supplies can be fully sequenced by a single LTC2924 and up to five supplies can be sequenced to a sixth master supply. The LTC2924 requires a minimum of external components, using only two feedback resistors per sequenced power supply and a single resistor to set hysteresis.

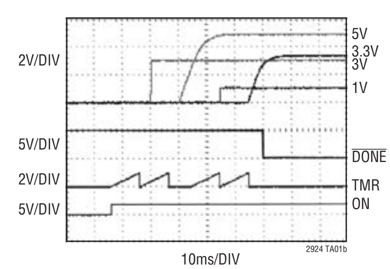
An internally regulated charge pump provides gate drive voltages for external logic and sub-logic-level MOSFETs. Adding a single capacitor enables an adjustable time delay between power supplies during both Power On and Power Off sequencing. A second capacitor can be added to enable a power good timer for detecting the failure of any power supply to turn on within the selected time. Errors in power supply sequencing and the control input are detected and reported at the FAULT output. The LTC2924 features precision input comparators which can provide 1% accuracy in monitoring power supply voltages.

Multiple LTC2924s may be easily cascaded to sequence a virtually unlimited number of power supplies.

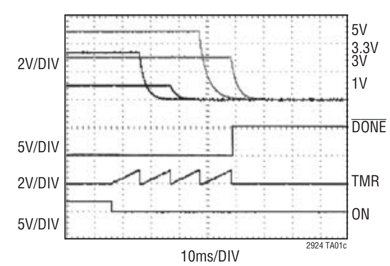
TYPICAL APPLICATION



Power-Up Sequence



Power-Down Sequence

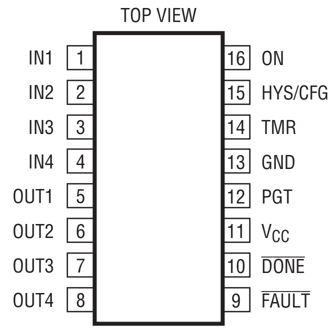


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) .... –0.3V to 6.5V
Input Voltages
  ON, IN1-IN4 ....–0.3V to V_{CC} + 0.3V
  PGT, TMR, HYS/CFG....................–0.3V to V_{CC} + 0.3V
Open-Drain Output Voltages
  $\overline{\text{FAULT}}$, $\overline{\text{DONE}}$ ....–0.3V to V_{CC} + 0.3V
Output Voltages
  (OUT1 - OUT4) (Note 5) .... –0.3V to V_{CC} + 4.5V
Operating Temperature Range
  LTC2924C .... 0°C to 70°C
  LTC2924I ....–40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)................... 300°C

PIN CONFIGURATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER INFORMATION

(http://www.linear.com/product/LTC2924#orderinfo)

Lead Free Finish

TUBE	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2924CGN#PBF	LTC2924CGN#TRPBF	2924	16-Lead Plastic SSOP	0°C to 70°C
LTC2924IGN#PBF	LTC2924IGN#TRPBF	2924I	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3V to 6V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
V_{CC}	Input Supply Range		●	3		6	V
I_{CC}	Input Supply Current		●		1.5	3	mA
ON Threshold							
$V_{ON(TH)}$	ON, Low to High Threshold		●	0.6000	0.6060	0.6121	V
$V_{OFF(TH)}$	ON, High to Low Threshold		●	0.6014	0.6074	0.6135	V
IN1-IN4 Threshold							
$V_{ON(TH)}$	IN1-IN4 Low to High Threshold		●	0.6020	0.6081	0.6142	V
$V_{OFF(TH)}$	IN1-IN4 High to Low Threshold		●	0.6026	0.6087	0.6148	V
ON, IN1-IN4 Characteristics							
V_{FAULT}	ON, IN1-IN4 High Speed Low Fault Threshold		●	0.33	0.4	0.48	V
$I_{ON(HYS)}$	ON, IN1-IN4 Hysteresis Current Range	$V_{ON} \geq V_{ON(TH)}$ (Note 2)	●	0.5		50	µA
$I_{ON(ERROR)}$	ON, IN1-IN4 Hysteresis Current Error	$1 – (I_{ON(HYS)}/(0.5/R_{HYS}))$, $V_{ON(TH)}$ = 1V 0.5µA ≤ I_{ON} < 25µA 25µA ≤ I_{ON} ≤ 50µA	 ● ●			 ±22 ±10	 % %
I_{LEAK}	ON, IN1-IN4 Leakage (Below Threshold)	$V_{ON(TH)}$ = 0.5V	●		2	±100	nA
$V_{ON(HYS)}$	ON, IN1-IN4 Minimum Hysteresis Voltage	$I_{HYS} \bullet R_{IN}$ (Note 6)	●	4			mV
OUT1-OUT4 Characteristics							
$V_{OUT(EN)}$	OUT1-OUT4 Gate Drive Voltage	I_{OUTn} = 0		V_{CC} + 4.5		V_{CC} + 6	V
$I_{OUT(EN)}$	OUT1-OUT4 On Current	OUT*n* On, $V_{OUT} = (V_{CC} + 4V)$	●	8.6	10	11.2	µA
$R_{OUT(OFF)}$	OUT1-OUT4 Off Resistance to GND	OUT*n* Off, I_{OUT} = 2mA	●			240	Ω
HYS Characteristics							
R_{HYS}	HYS Current Programming Resistor Range	(Notes 2, 3)		10k		1M	Ω
V_{HYS}	HYS Programming Voltage	R_{HYS} Tied to GND R_{HYS} Tied to V_{CC}			0.5 V_{CC} – 0.5		V V
TMR Characteristics							
I_{TMR}	Timer Pin Output Current	Timer On, $V_{TMR} \leq$ 0.9V	●	4	5	6	µA
$V_{TH(HI)}$	Timer High Voltage Threshold	V_{CC} = 5V		0.93	1	1.07	V
PGT Characteristics							
I_{PGT}	Power Good Timer Pin Output Current	Power Good Timer On, $V_{PGT} \leq$ 0.9V	●	4	5	6	µA
V_{PGT}	Power Good Timer Fault Detected Voltage Threshold	V_{CC} = 5V		0.93	1	1.07	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3V to 6V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{\text{DONE}}$ Characteristics							
$R_{D(LO)}$	$\overline{\text{DONE}}$ Pin Pull-Down Resistance to GND	$\overline{\text{DONE}}$ = Low, I = 2mA	●			100	Ω
$I_{D(HI)}$	$\overline{\text{DONE}}$ Pin Off Leakage Current	$\overline{\text{DONE}}$ = High	●			15	µA
$\overline{\text{FAULT}}$ Characteristics							
$R_{FAULT\ (LO)}$	$\overline{\text{FAULT}}$ Pin Pull-Down Resistance to GND	$\overline{\text{FAULT}}$ Being Pulled Low Internally, I = 2mA	●			400	Ω
$I_{FAULT(HI)}$	$\overline{\text{FAULT}}$ Pin Off Leakage Current	$\overline{\text{FAULT}}$ High	●			2	µA
$V_{FAULT(HI)}$	Voltage Above Which an Externally Generated FAULT Condition Will Not be Detected		●	1.6			V
$V_{FAULT(LO)}$	Voltage Below Which an Externally Generated		●			0.6	V
	FAULT Condition Will be Detected						
$R_{F(EXT)}$	External Pull-Up Resistance		●	10			kΩ
t_{FAULT}	Externally Commanded FAULT Below $V_{FAULT(LO)}$ to OUT1-OUT4 Pull-Down On Delay		●			1	µs
$t_{FAULT(MIN)}$	Externally Commanded FAULT Minimum Time Below $V_{FAULT(LO)}$	(Note 4)		1			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Hysteresis current must be 500nA minimum. Hysteresis current may exceed 50µA, but accuracy is not guaranteed.

Note 3: HYS/CFG pin must be pulled to GND or V_{CC} with an external resistor. See Applications Information for details.

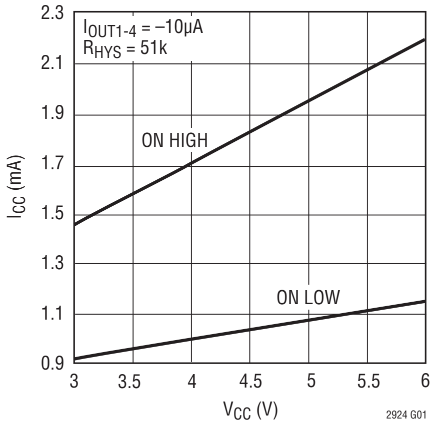
Note 4: Determined by design, not production tested. External circuits pulling down on the $\overline{\text{FAULT}}$ pin must maintain the signal below $V_{FAULT(LO)}$ for ≥1µs.

Note 5: Internal circuits may drive the OUT*n* pins higher than the Absolute Maximum Ratings.

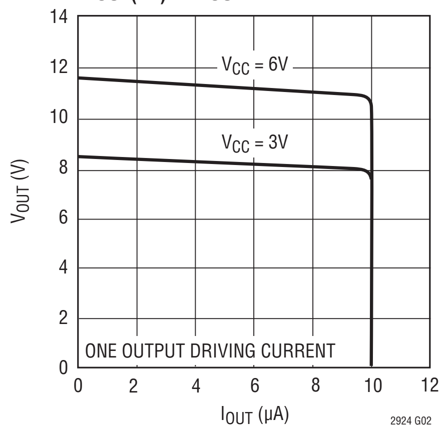
Note 6: R_{IN} is the parallel combination of the two resistors forming the resistive divider connected to the ON and IN1-IN4 pins.

TYPICAL PERFORMANCE CHARACTERISTICS

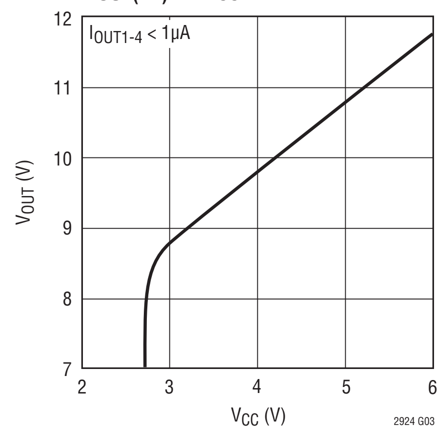
I_{CC} vs V_{CC}



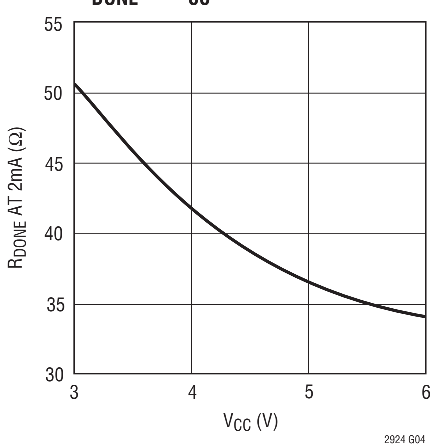
$V_{OUT(EN)}$ vs I_{OUT}



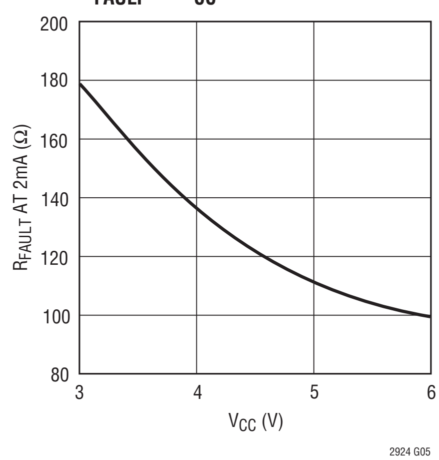
$V_{OUT(EN)}$ vs V_{CC}



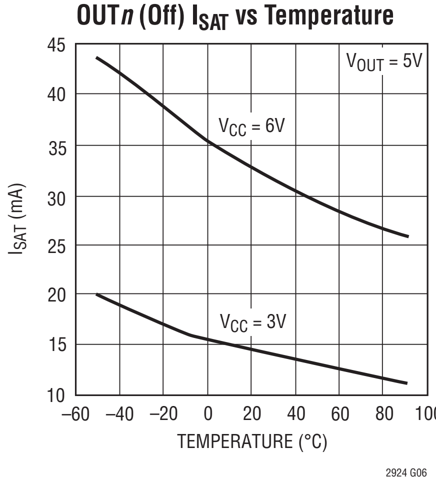
R_{DONE} vs V_{CC}



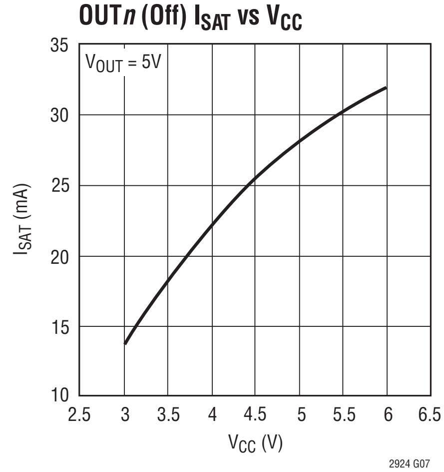
R_{FAULT} vs V_{CC}



OUT*n* (Off) I_{SAT} vs Temperature



OUT*n* (Off) I_{SAT} vs V_{CC}



PIN FUNCTIONS

IN1-IN4 (Pins 1, 2, 3, 4): Sequenced Power Supply Monitor Input. Connect this pin to an external resistive divider between each sequenced power supply and GND. During Power On sequencing, 0.61V (typ) at this pin indicates that the sequenced power supply (enabled with each of the OUT1-OUT4 pins) has reached the desired Power On sequence voltage. A hysteresis current (programmed by the HYS pin) is sourced out of each of the IN1-IN4 pins after the 0.61V threshold is detected. During the Power Off sequence, 0.61V at this pin indicates that the sequenced power supply has reached the desired Power Off voltage. The hysteresis current is removed after the 0.61V threshold is detected.

OUT1-OUT4 (Pins 5, 6, 7, 8): Sequenced Power Supply Enable. Connect this pin to the shutdown pin or an external series N-channel MOSFET gate for each power supply being sequenced. (A low at this pin means the sequenced power supply is commanded to turn off.) When disabled, each output is connected to GND with a resistance of <240Ω. When enabled, each output is connected to an internally generated charge pump supply (nominally V_{CC} + 5V) via an internal 10µA (typ) current source.

$\overline{\text{FAULT}}$ (Pin 9): Fault Pin. Pull this pin high with an external 10k resistor. The LTC2924 will pull this pin low if a fault condition is detected (see Applications Information for details). Pulling this pin low externally causes a simultaneous unsequenced Power Off.

$\overline{\text{DONE}}$ (Pin 10): Done Pin. Pull this pin to V_{CC} with an external 10k resistor. This open-drain output pulls low at the completion of the Power-On sequence. At the end of the Power Off sequence, the LTC2924 floats this pin. For cascading multiple LTC2924s, see Application Information for connecting the $\overline{\text{DONE}}$ pin.

V_{CC} (Pin 11): LTC2924 Power Supply Input. All internal circuits are powered from this pin. V_{CC} should be connected to a low noise power supply voltage and should be bypassed with at least a 0.1µF capacitor to the GND pin in close proximity to the LTC2924.

PGT (Pin 12): Power Good Timer. The PGT pin sets the time allowed for a power supply to turn on after being enabled with the OUT1-OUT4 pins. Connecting a capacitor between this pin and ground programs a 200mS/µF duration. The PGT pin is reset before each of the OUT1-OUT4 pins are asserted. If the voltage at the PGT pin reaches 1V, a fault condition is asserted. The PGT pin must be connected directly to ground to disable the power good timer function. Keep the ratio C_{PGT}/C_{TMR} between 1 and 100.

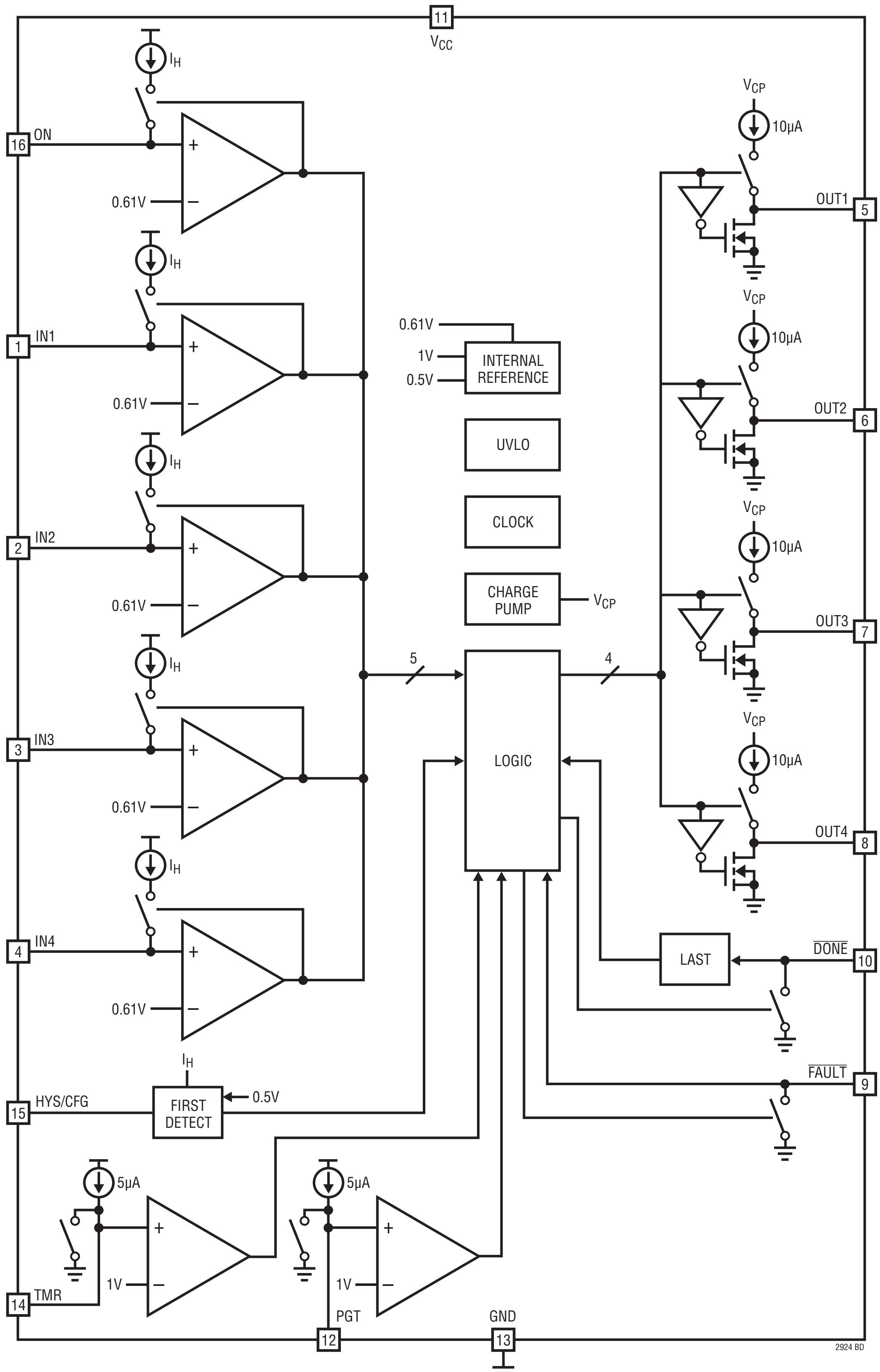
GND (Pin 13): Ground. All internal circuits are returned to the GND pin. Connect this pin to the ground of the power supplies that are being sequenced.

TMR (Pin 14): Timer. A capacitor connected between this pin and ground sets the time delay between a supply ready (IN1-IN4) signal and the enabling of the next power supply in the sequence (OUT1-OUT4), with a 200mS/µF duration. The TMR pin may be left floating if no delay is required between supplies being sequenced on or off. The PGT pin should be grounded if the TMR pin is left floating. If an internal fault condition occurs, TMR will indicate so by going to V_{CC} until the fault condition is cleared. Do not connect any other circuits to the TMR pin.

HYS/CFG (Pin 15): Hysteresis Current Setting and Cascade Configuration. Connecting a resistor between this pin and GND programs a $0.5/R_{EXT}$ (typ) hysteresis current which is sourced out of each IN and ON pin. When multiple LTC2924s are cascaded, the HYS/CFG pin is also used to configure the position of the *first* LTC2924. See Applications Information for details.

ON (Pin 16): On Pin. Commands the LTC2924 to sequence the power supplies up (Power On sequence) or down (Power Off sequence). Typically connected to a system controller. Hysteresis current is applied to this pin when above 0.61V (typ). This pin has a precision 0.61V threshold and can be used to sense a nonsequenced power supply's voltage to start the Power On sequence. See Applications Information for details. For cascading multiple LTC2924s, see Applications Information for connecting the ON pin.

FUNCTIONAL DIAGRAM



OPERATION

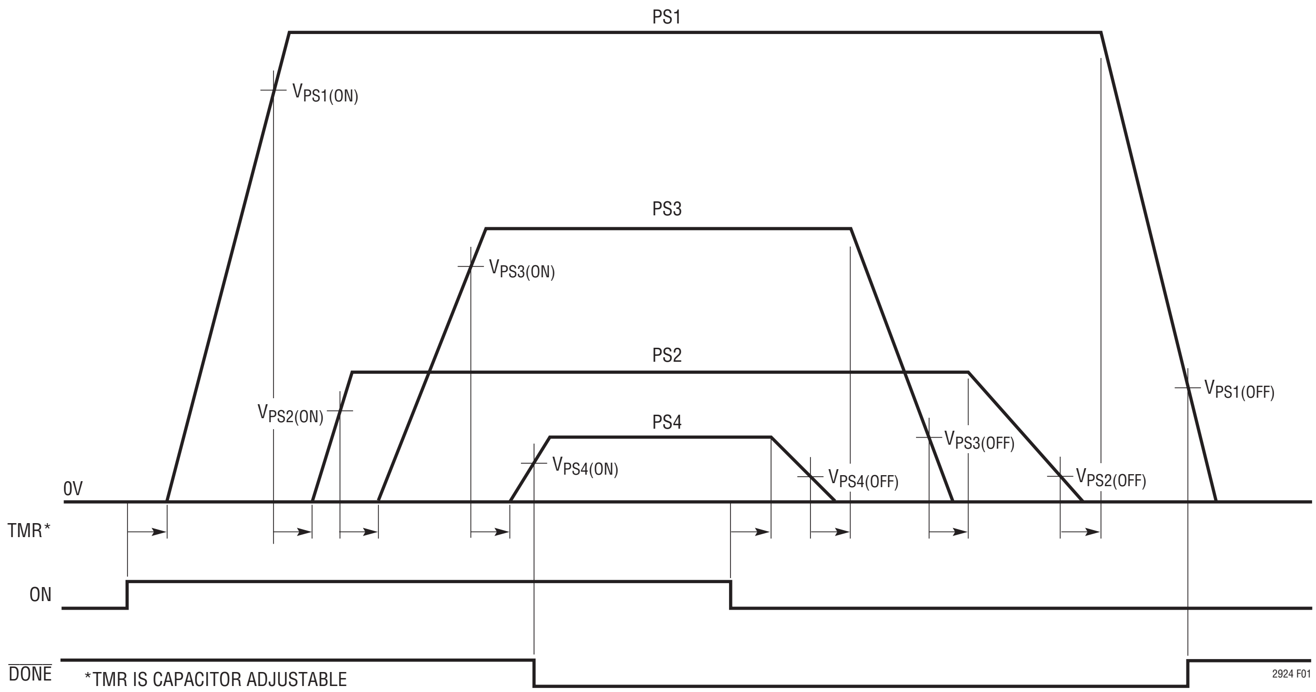


Figure 1. Power On and Power Off Sequence for Four Supplies

The LTC2924 is a power supply sequencer designed for use with external N-channel MOSFETs or power supplies with shutdown pins. Four power supplies can be fully sequenced by a single LTC2924 (see Figure 1). An internally regulated charge pump provides (V_{CC} + 5V) gate voltages for driving external logic-level and sub-logic level MOSFETs. Adding a single capacitor enables an adjustable time delay between power supplies during both Power On and Power Off sequencing. A second capacitor can be added to enable a power good timer which detects the failure of any power supply to turn on within the set time.

The ON pin signal is used to command the LTC2924 to start the Power On and Power Down sequences. To command the Power On sequence, the ON pin is pulled above 0.61V by a system controller or a resistive divider from a power supply. A voltage comparator senses the ON command and signals the sequencing logic to start the Power On sequence.

When the Power On sequence starts, the TMR grounding switch is released and a 5µA current source charges an external capacitor, C_{TMR} (see Figure 2). When the voltage on this capacitor exceeds 1V, a comparator signals the

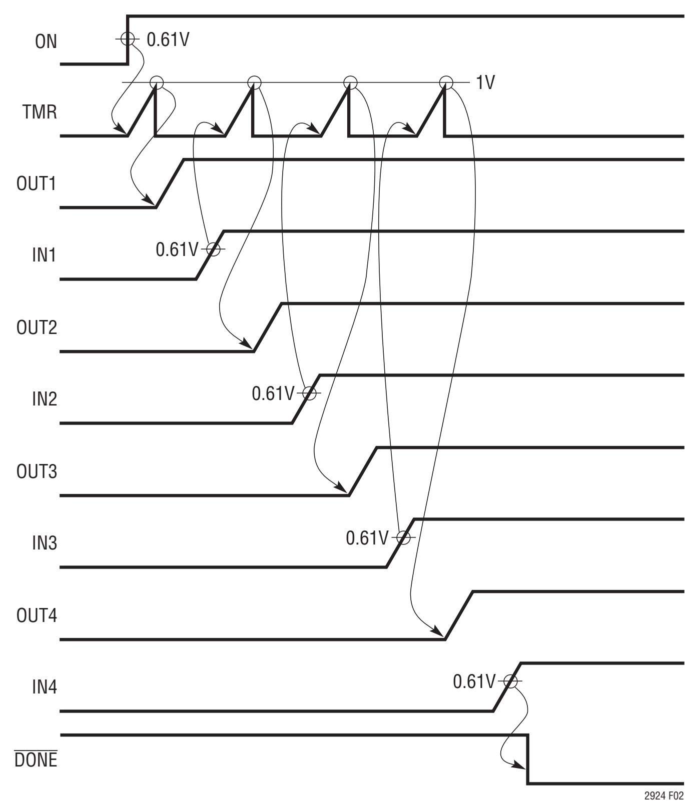


Figure 2. On Sequence for Four Supplies

OPERATION

logic, which starts the charge pump and enables OUT1 to turn on the first power supply. The power good timer circuit is also enabled by turning off the switch that is shorting the external capacitor to ground and enabling a 5µA current source to charge the C_{PGT} capacitor.

The output circuit responds by opening a switch, which is shorting the OUT1 pin to ground and enabling a 10µA current source, which is connected to the charge pump. The OUT1 pin can be connected to either the shutdown pin of a power supply or the gate of a N-channel MOSFET that is in series with the output of the sequenced power supply.

As the power supply turns on, the resistive divider connected to the IN1 pin starts to drive up the voltage at the IN1 pin. When the voltage at this pin exceeds 0.61V, the comparator signals the logic that the first power supply is on. At this time a current is sourced out of the IN1 pin which serves as the hysteresis current for the input comparator. This allows the application to choose a lower Power Off voltage sense during the Power Off sequence. The power good timer (PGT) circuit is signaled and resets the PGT capacitor. The timer circuit is enabled and the cycle repeats until the last power supply has turned on.

When the last power supply has turned on, the $\overline{\text{DONE}}$ pin pull-down switch is turned on to signal that the Power On sequence has completed.

If a power supply fails to turn on after it is enabled and the voltage at the PGT pin exceeds 1V, the LTC2924 will disable all power supplies by pulling all OUT pins to ground. A fault condition will be indicated by the $\overline{\text{FAULT}}$ pin pulling low.

The hysteresis current sourced at the ON pin and each IN pin is set at the HYS/CFG pin. The current is determined by an external resistor nominally pulled to ground. The hysteresis current is $0.5V/R_{HYS}$.

The Power Off sequence is initiated by pulling the ON pin below 0.61V after a Power On sequence has completed (see Figure 3). The Power Off sequence turns off the power supplies in the reverse order of the Power On sequence. OUT4 is turned off first. The timer function is used between each supply being sequenced down. The PGT is not used. The end of the Power Off sequence is indicated by the LTC2924 floating the $\overline{\text{DONE}}$ pin.

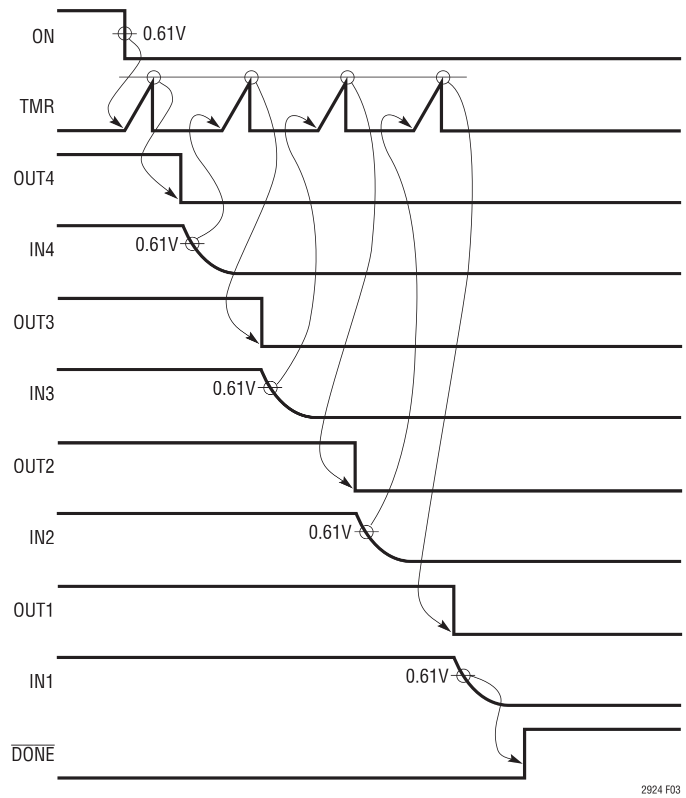


Figure 3. 4-Power Supply Power Off Sequence

APPLICATIONS INFORMATION

Up to five supplies can be sequenced to a sixth master supply by a single LTC2924 (Figure 4). The turn on of the first power supply is sensed by the ON pin. Power supplies two through five are enabled by the OUT1 through OUT4 pins, and their turn on sensed by the IN1 through IN4 pins respectively. The last power supply is enabled by the $\overline{\text{DONE}}$ pin, which is generally connected through an inverter. This application is used where power supplies are sequentially sequenced on and the turn off is simultaneous. Multiple LTC2924s can be cascaded to facilitate sequencing of eight or more power supplies. See the Cascading Multiple LTC2924s section.

Selecting the Hysteresis Current and IN Pin Feedback Resistors

The IN1-IN4 pins are connected to a sequenced power supply with a resistive divider. The resistors are calculated by first selecting a hysteresis current, I_{HYS}, and calculating R_{HYS}:

$$R_{HYS} = \frac{0.5V}{I_{HYS}}; 0.5\mu A \le I_{HYS} \le 50\mu A$$

For each sequenced power supply, choose a voltage when the power supply is considered to be On during

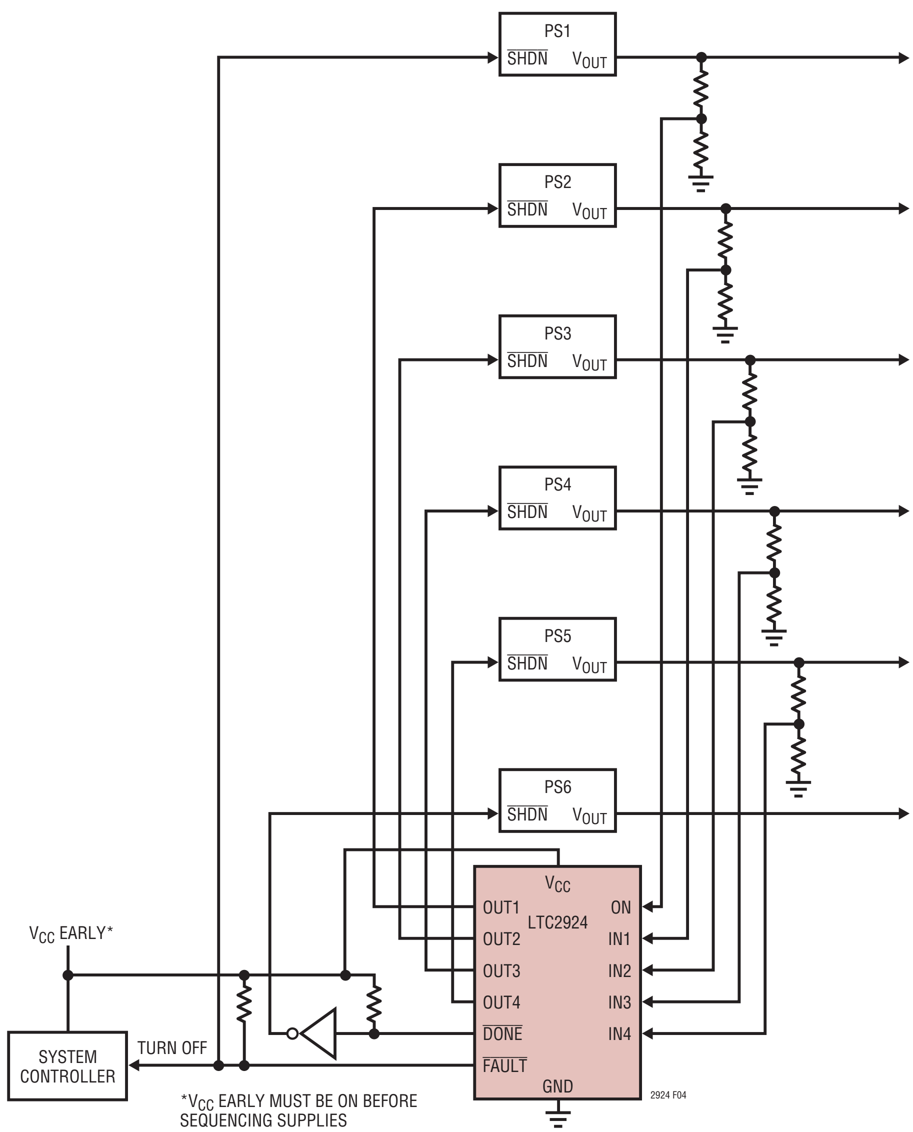


Figure 4. 6-Power Supply Sequencer Block Diagram

APPLICATIONS INFORMATION

a Power On sequence (V_{ON}) and Off during a Power Off sequence (V_{OFF}).

Referring to Figures 5 and 6, each set of resistors can then be calculated by:

$$R_B = \frac{V_{ON} - V_{OFF}}{I_{HYS}}$$

$$R_A = \frac{R_B \cdot 0.61V}{V_{ON} - 0.61V}$$

In the following example (Figure 5) I_{HYS} is 50µA. This corresponds to a R_{HYS} resistor of:

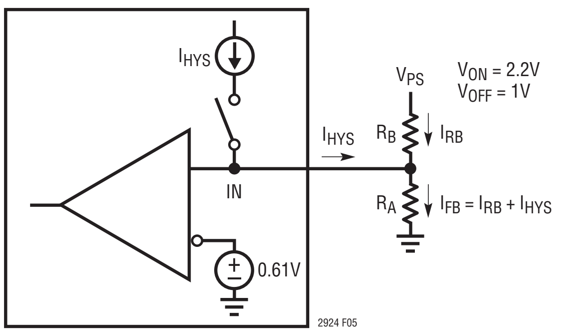


Figure 5. Designing I_{HYS}, Feedback Resistors

$$R_{HYS} = \frac{0.5V}{50\mu A} = 10k\Omega$$

In Figure 5, V_{ON} = 2.2V and V_{OFF} = 1V. Using the equations provided above:

$$R_B = \frac{2.2V - 1V}{50\mu A} = 24k\Omega$$

$$R_A = \frac{24k\Omega \cdot 0.61V}{2.2V - 0.61V} = 9.2k\Omega$$

Hysteresis Voltage Check

After calculating the resistors R_B and R_A, check to make sure the hystersis voltage at the ON and IN1-IN4 pins is greater than 4mV. Use the following equation:

$$V_{HYS} = \frac{(V_{ON} - V_{OFF}) \cdot R_A}{R_A + R_B}$$

For this example:

$$V_{HYS} = \frac{(2.2V - 1V) \cdot 9.2k\Omega}{9.2k\Omega + 24k\Omega} = 0.33V$$

which is greater than 4mV.

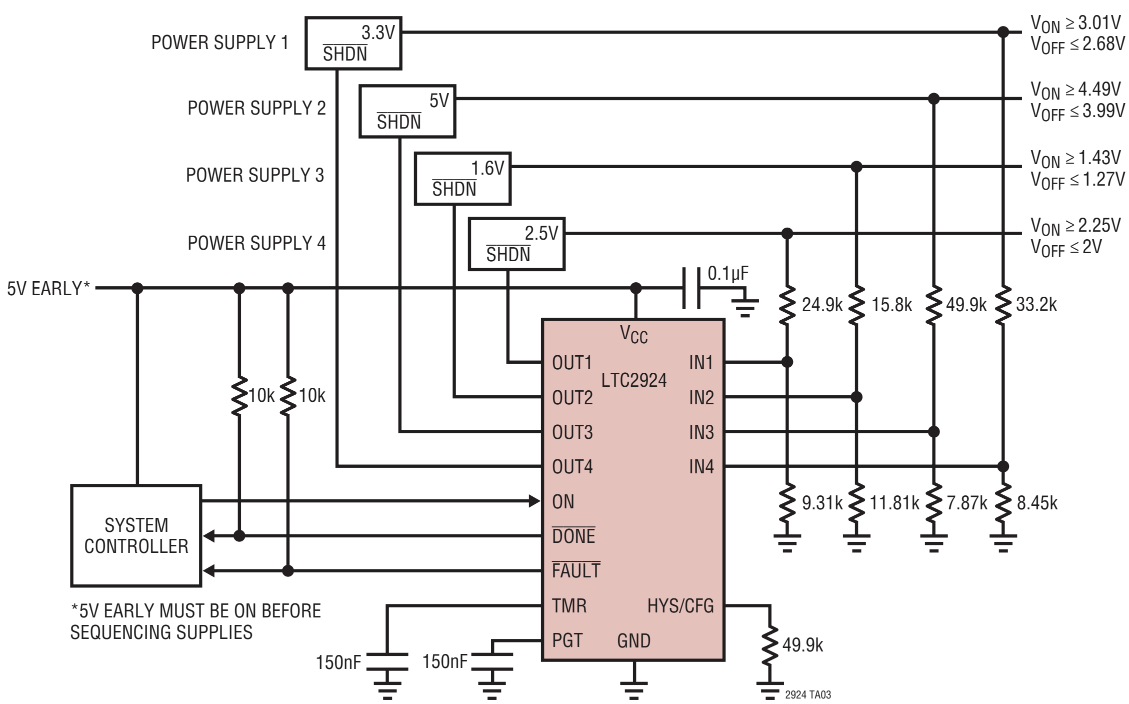


Figure 6. Typical Power Supply Sequencer

APPLICATIONS INFORMATION

Minimize stray capacitance on the ON and IN1-IN4 pins. As a practical matter, lay out these resistors as close to the LTC2924 as possible.

Details of Resistor Calculations

In this example, the voltage at the IN pins is 0.61V when the LTC2924 detects that the power supply is On during a Power On sequence or Off during a Power Off sequence.

The delta voltage, ΔV, represents the difference:

$$\Delta V = 2.2V - 1V = 1.2V$$

This delta voltage on R_B will be equal to the product of hysteresis current I_{HYS} and R_B. Therefore:

$$R_B = \Delta \frac{\Delta V}{I_{HYS}} = \frac{1.2V}{50\mu A} = 24k\Omega$$

The current I_{RB} at the Power On voltage of 2.2V is:

$$I_{RB} = \frac{2.2V - 0.61V}{24k} = 66\mu A$$

During the Power On sequence, $I_{HYS} = 0$, so I_{FB} is equal to I_{RB} and R_A is:

$$R_A = \frac{0.61}{66\mu A} = 9.2k$$

V_{OFF} Precaution

Use caution if designs call for V_{OFF} voltages less than ~0.8V. Many loads stop using significant current at this level, and the power supply may take a long time to go below this voltage. If V_{OFF} voltages at or less than this voltage are necessary, consider adding an extra resistive load at the output of the power supply to ensure it discharges in a reasonable amount of time.

Selecting the Timing Capacitor

During the Power On sequence, the timer is used to create a delay between the time one supply reaches the On threshold and the next supply is enabled. During the Power Off sequence, the timer is used to create a delay between the time one supply reaches the Off threshold and the next supply is disabled. Select the timing capacitor with the following equation:

$$C_{TMR}\ [\mu F] = t_{DELAY} \bullet 5\mu F/s$$

Leaving the TMR pin unconnected will generate the minimum delay. If the TMR pin is unconnected then the PGT pin should be grounded. The accuracy of the time delay will be affected by the capacitor leakage (the nominal charge current is 5µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

Selecting the Power Good Timer (PGT) Capacitor

During the Power On sequence, the PGT can be used to detect the failure of a power supply to reach the desired On voltage. The PGT is enabled each time a power supply is enabled by the OUT1-OUT4 pins. The PGT is reset each time an IN1-IN4 pin detects that a power supply is at the desired On voltage. Select the PGT timeout capacitor with the following equation:

$$C_{PGT}\ [\mu F] = t_{PGT} \bullet 5\mu F/s$$

If no PGT is desired, the PGT pin must be shorted to ground. The accuracy of the PGT timeout will be affected by the capacitor leakage (the nominal charge current is 5µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended. The ratio of C_{PGT}/C_{TMR} should be kept between 1 and 100. If a C_{PGT} value is required that exceeds the maximum ratio of C_{PGT}/C_{TMR} then C_{TMR} should be increased appropriately.

APPLICATIONS INFORMATION

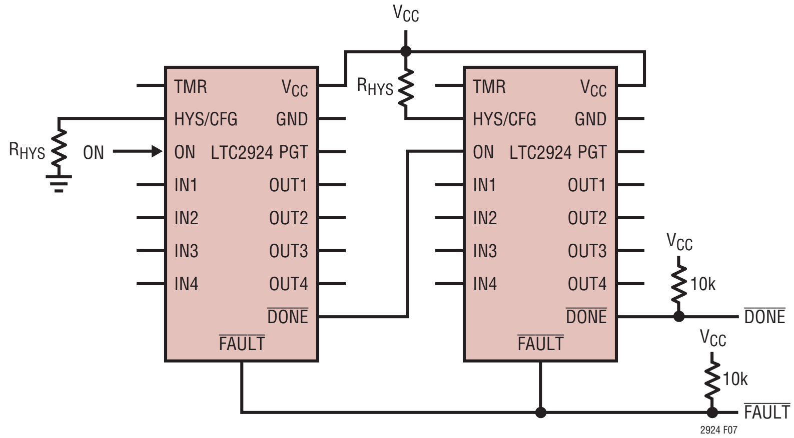


Figure 7. Cascading Two LTC2924s to Fully Sequence Up to Eight Power Supplies

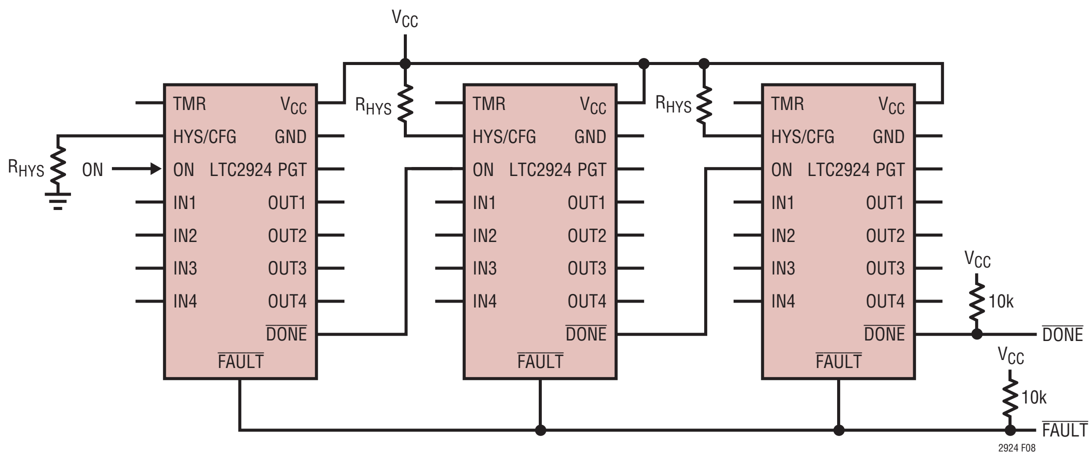


Figure 8. Cascading Three LTC2924s to Fully Sequence Up to 12 Power Supplies

Cascading Multiple LTC2924s

Two or more LTC2924s may be cascaded to fully sequence 8,12 or more power supplies. Figures 7 and 8 show how to configure the LTC2924 to sequence 8 and 12 power supplies. To sequence more power supplies, use the circuit in Figure 8 and add more LTC2924s in the middle.

Notice that the *last* LTC2924 in the cascade string must have a pull-up resistor on the $\overline{\text{DONE}}$ pin. Any LTC2924 that is not the *first* in the cascade string should have the hysteresis current setting resistor, R_{HYS}, pulled to V_{CC} instead of ground. The value of the R_{HYS} resistor remains unchanged. The $\overline{\text{FAULT}}$ pins should all be connected together and pulled up with a single 10k resistor.

Care should be taken when designing a circuit cascading multiple LTC2924s. Use the following guidelines:

- All V_{CC} and ground pins for the LTC2924s in the cascade chain must be connected to the same power supply.
- The ground pins should be connected via a ground plane.
- Cascaded LTC2924s communicate using a combination of levels and pulses which do not look like the normal output of a $\overline{\text{DONE}}$ pin nor input to an ON pin. **Do not connect any other components to the node between the $\overline{\text{DONE}}$ and ON pins.** Keep the parasitic capacitance on this node below 75pF. Care should be taken when routing a circuit trace between $\overline{\text{DONE}}$ and ON. If possible, run the trace adjacent to the ground plane, and/or shield the trace with a ground trace on either side. Leakage currents must be maintained below 2μA on this node.

APPLICATIONS INFORMATION

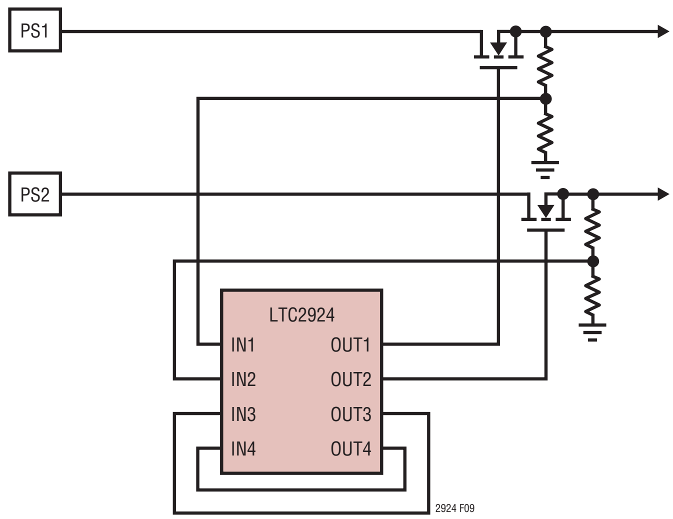


Figure 9. Connecting Unused OUT and IN Pins

Connecting Unused OUT and IN Pins

Figure 9 shows how to connect unused OUT and IN pins on the LTC2924. Unused OUT-IN pairs must be connected together to ensure proper operation.

Fault Detection

The LTC2924 has sophisticated fault detection which can detect:

- Power On and Power Off sequence errors
- System controller command errors
- Power On timeout failure (with the power good timer enabled)
- Externally commanded faults ($\overline{\text{FAULT}}$ pin pulled low)

If any of the above faults are detected, the LTC2924 **immediately pulls the OUT1-OUT4 pins low turning off all of the power supplies.** If the fault condition is detected in one of the supplies controlled by the LTC2924 (an "internally generated" fault), the $\overline{\text{FAULT}}$ pin is immediately pulled low indicating the fault condition.

Clearing the Fault Condition

In order to clear the fault condition within the LTC2924, the following conditions must exist:

- All four IN pins must be below 0.61V
- The ON pin must be below 0.61V
- In the case of an externally generated fault, the $\overline{\text{FAULT}}$ pin must not be pulled down.

Fault Condition Indicator

If the LTC2924 receives a commanded fault (a cascaded LTC2924 or an external source pulls down on the $\overline{\text{FAULT}}$ pin) the LTC2924 will pull the TMR pin low. If the LTC2924 has detected the fault itself (from its internal fault detection circuits) it will indicate so by raising the TMR pin to V_{CC}. This internal/external fault indicator can be especially helpful while searching for the source of a fault condition when multiple LTC2924s are cascaded.

If a fault occurs when the ON pin is high, the fault status indication on the TMR pin will remain valid until the ON pin goes low.

APPLICATIONS INFORMATION

Note that the TMR pin may take a while to reach the V_{CC} voltage. The pin is pulled to V_{CC} with the same 5µA current source used for the TMR function. The larger the timer capacitor, the longer this will take. To estimate the amount of time required for the TMR pin to reach V_{CC} in a fault condition, multiply the normal timer duration by V_{CC} (in Volts). See Figures 7 and 8 for $\overline{\text{FAULT}}$ pin connections when two or more LTC2924 chips are cascaded.

Sequence Errors

The LTC2924 keeps track of power supplies that should be on during the Power On sequence and the Power Off sequence. The LTC2924 also monitors each IN pin after all of the power supplies have sequenced on. If a power supply (as monitored at the IN1-IN4 pins) goes low when it should be high, a fault condition is detected. All four OUT pins are pulled low and the $\overline{\text{FAULT}}$ pin will be pulled low.

The precision voltage threshold for detection of a sequence error at any of the IN1-IN4 pins is the same as the normal threshold (~0.61V). The precision voltage comparators used in the LTC2924 employ a sampled technique to improve accuracy. The sample time is approximately 20µs. To improve the speed of detection for a sequence error, a second high speed comparator is used for detecting a low power supply. The voltage threshold for the high speed comparators is approximately 0.4V ($V_{ON(FAULT)}$). Voltages sensed below this threshold when a power supply should be ON will cause a fault in ~1µs.

System Controller ON Command Errors

Once the LTC2924 receives the Power On command via the ON pin, the ON pin must remain above 0.61V until the Power On sequence has completed (e.g. $\overline{\text{DONE}}$ is asserted). Removing the ON command before the LTC2924 Power On sequence has completed is considered a fault condition. All of the OUT1-OUT4 pins that are already high will be pulled low and the $\overline{\text{FAULT}}$ pin will be pulled low.

The same is true for the Power Off sequence. If the LTC2924 has completed the Power On sequence and the ON pin goes low, the ON pin must remain below 0.61V until the Power Off sequence has completed. Raising the ON pin above 0.61V before the Power Off sequence has completed is considered a fault condition. Any OUT*n* pins that are still high will immediately be pulled low and the $\overline{\text{FAULT}}$ pin will be pulled low.

Power On Timeout Errors

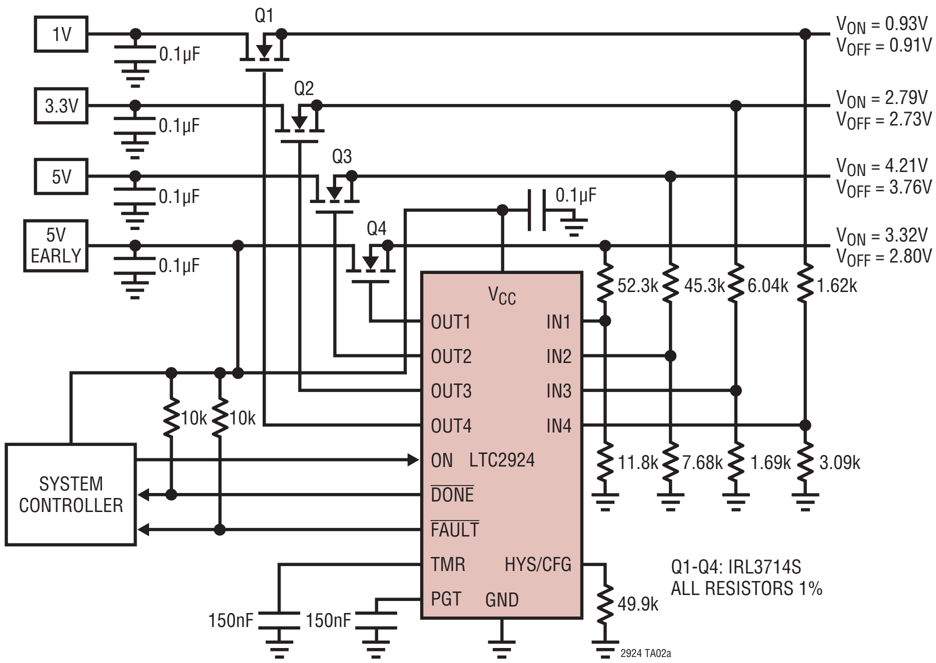
If the LTC2924 PGT is being used (not tied to ground) a fault condition will be detected when the PGT pin goes above ~1V. If this occurs during Power On, all of the OUT1-OUT4 pins that are already high will be pulled low and the $\overline{\text{FAULT}}$ pin will be pulled low.

Externally Commanded Faults

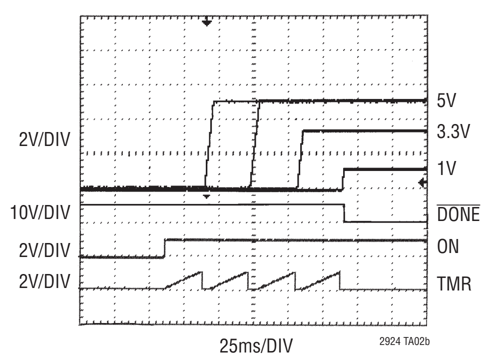
If an external circuit pulls the $\overline{\text{FAULT}}$ pin low, an external fault condition is detected and all OUT pins will be pulled low. After sensing the Externally Commanded Fault, the LTC2924 will also pull down on the $\overline{\text{FAULT}}$ pin until the conditions for clearing the fault condition exist (see Clearing the Fault Condition).

TYPICAL APPLICATIONS

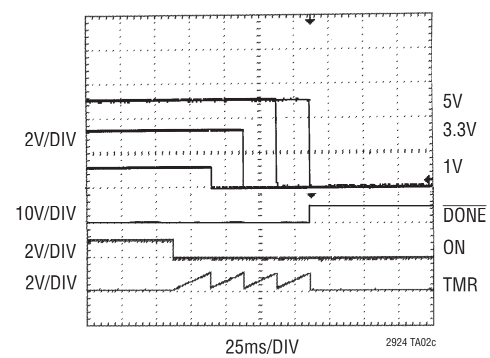
Series MOSFET Power Supply Sequencer



Power-Up Sequence

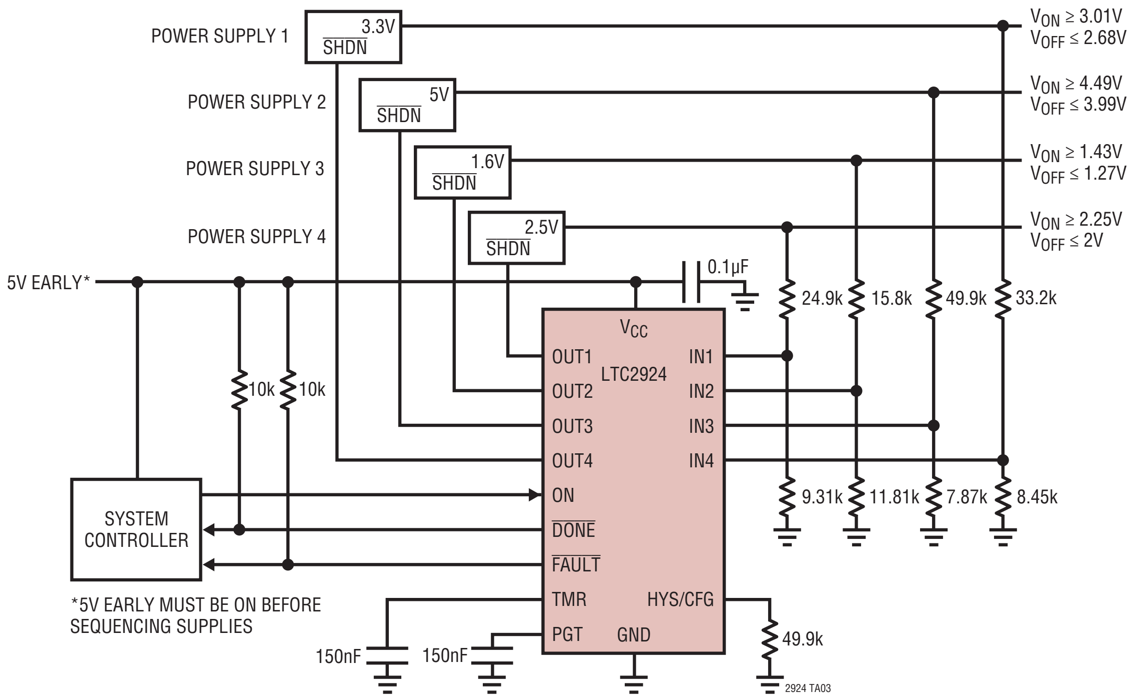


Power-Down Sequence



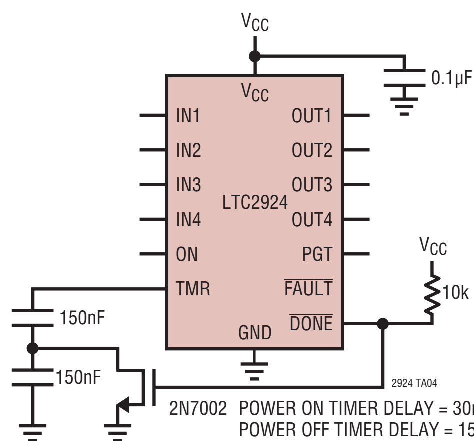
TYPICAL APPLICATIONS

Shutdown Pin Power Supply Sequencer



*5V EARLY MUST BE ON BEFORE SEQUENCING SUPPLIES

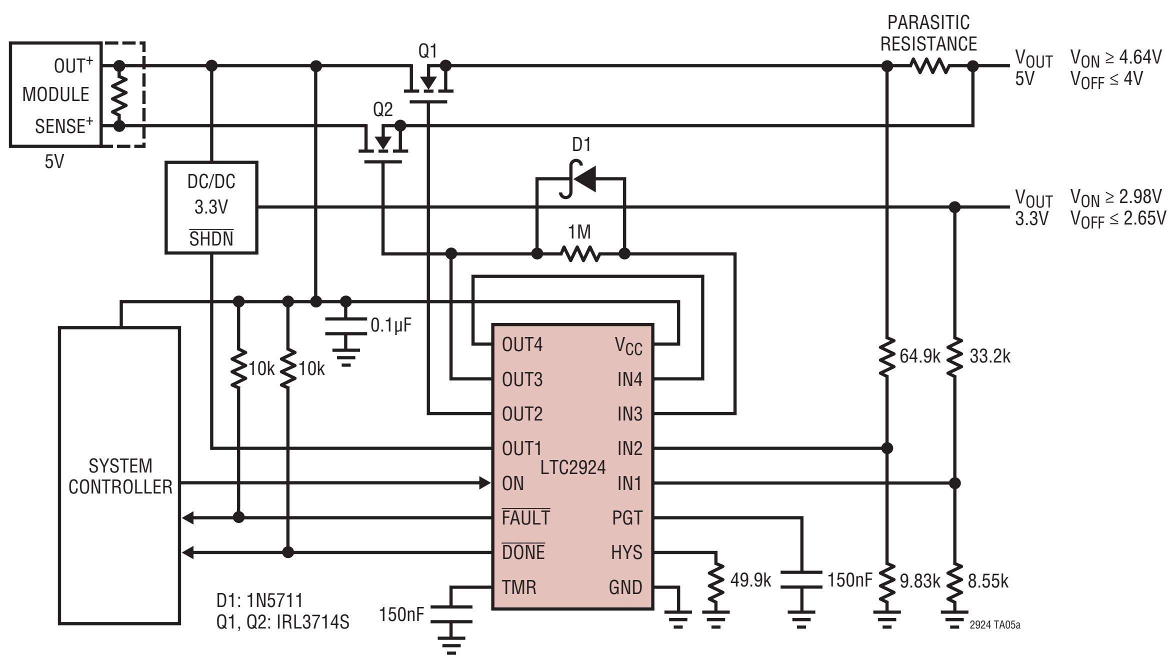
Power On Sequence Timer Delay Longer than Power Off Sequence Timer Delay



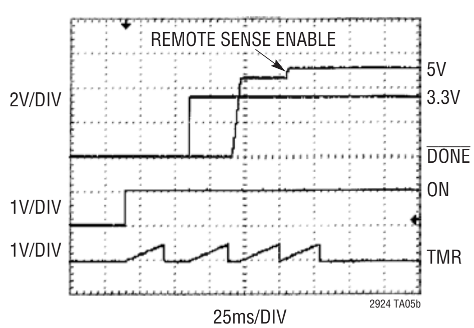
POWER ON TIMER DELAY = 30ms
POWER OFF TIMER DELAY = 15ms

TYPICAL APPLICATIONS

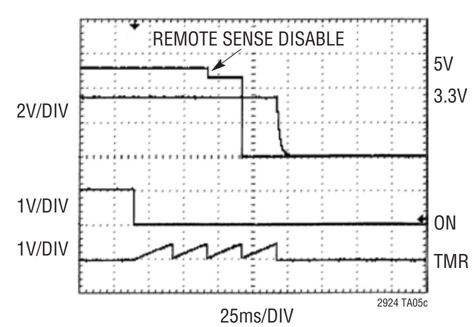
2-Supply Sequencer with Delayed Sense Pin, One Channel Unused



Power-On

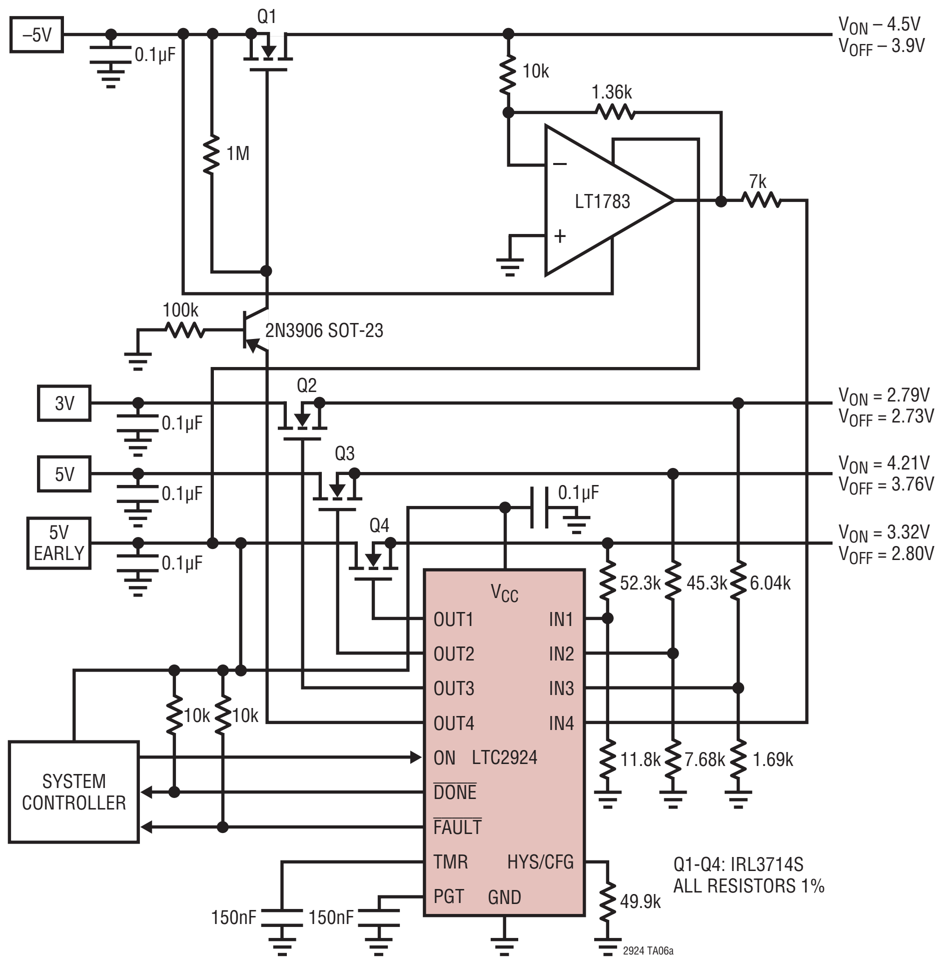


Power-Off

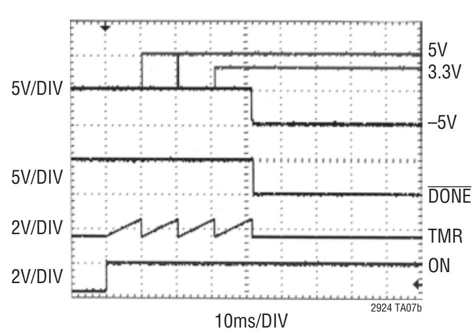


TYPICAL APPLICATIONS

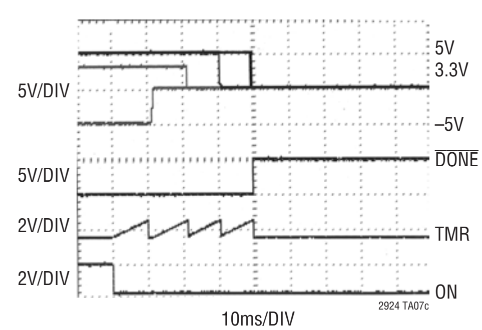
Precision Negative Rail Sequencer



Power-Up Sequence



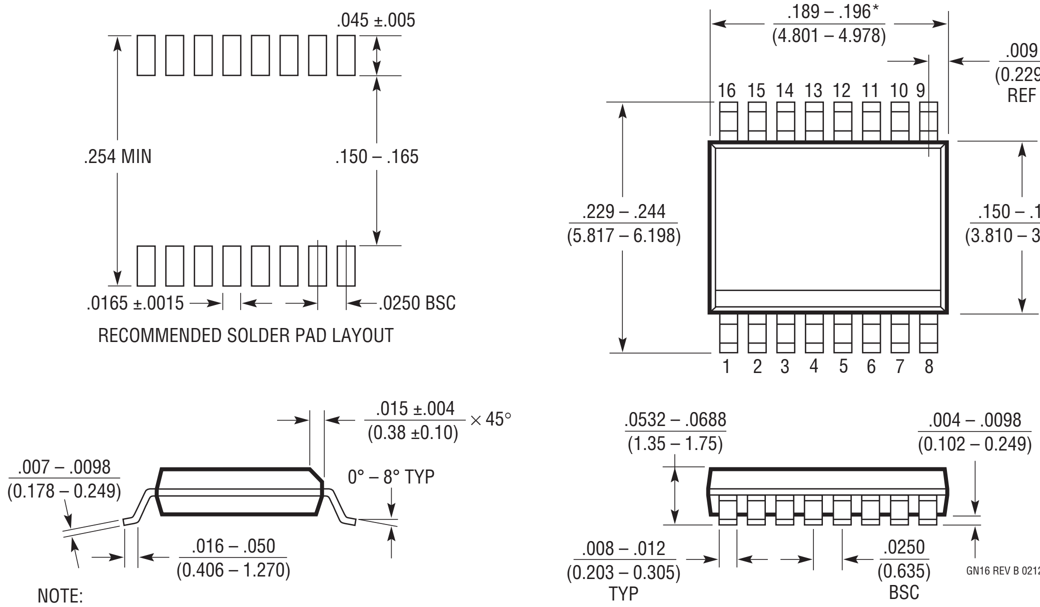
Power-Down Sequence



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2924#packaging for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

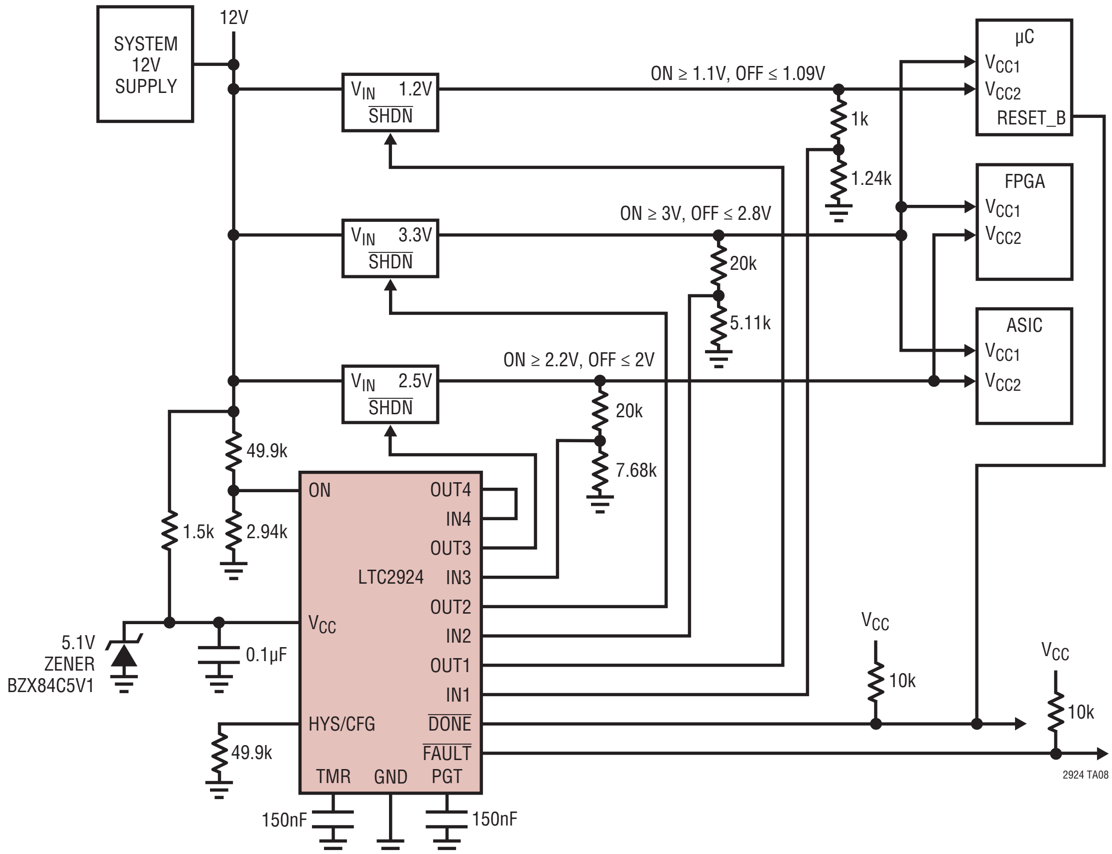
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	02/12	Updated PGT and TMR pin descriptions in Pin Functions.	6
		Updated Selecting the Timing Capacitor and Selecting the Power Good Timer (PGT) Capacitor sections of Applications Information.	12
		Revision to Typical Application drawing TA06a.	19
C	02/16	Removed Lead Finish Part Numbers	2
		Updated GN Package Drawing	20

TYPICAL APPLICATION

12V 3-Supply Sequencer with LTC2924 Power Supplied by a Zener Shunt Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2920-1/LTC2920-2	Single/Dual Power Supply Margining Controller	Symmetric/Asymmetric High and Low Voltage Margining
LTC2921/LTC2922	Power Supply Tracker with Input Monitors	3 (LTC2921) or 5 (LTC2922) Remote Sense Switching
LTC2923	Power Supply Tracking Controller	Up to 3 Supplies
LTC2925	Multiple Power Supply Tracking Controller	Power Good Timer, Remote Sense Switch
LTC2926	MOSFET Controlled Power Supply Tracker	Closed Loop (Feedback) Tracking for 3 Supplies
LTC2927	Single Power Supply Tracker	For Point of Load or Distributed Applications

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 ● FAX: (408) 434-0507 ● www.linear.com
LT 0216 REV C • PRINTED IN USA