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# FSUSB63 — 3:1 High-Speed USB 2.0 Switch / Multiplexer

## Features

Switch Type	3:1 USB Switch
USB	USB 2.0 High-Speed & Full-Speed Compliant
Break-Before-Make Time	126µs
R <sub>ON</sub>	6Ω Typical
C <sub>ON</sub>	6pF Typical
Bandwidth	830MHz
V <sub>CC</sub>	2.7 to 4.4V
V <sub>CNTRL</sub>	0 to V <sub>CC</sub>
Operating Temperature	-40°C to 85°C
I <sub>CCSLP</sub>	<1µA
I <sub>CCACT</sub>	7.5µA Typical
Package	12- Lead UMLP 1.80 x 1.80 x 0.55mm, 0.40mm pitch
Top Mark	KG
Ordering Information	FSUSB63UMX

## Applications

- Cell Phone, Digital Camera, Notebook
- LCD Monitor, TV, and Set-Top Box
- Netbook, Mobile Internet Device (MID)

## Description

The FSUSB63 is a bi-directional, low-power, High-Speed (HS) USB 2.0 3:1 Multiplexer (MUX). It is optimized for switching among three high-speed (480Mbps) sources or any combination of high-speed and full-speed (12Mbps) USB sources, such as an application processor, to one USB 2.0 connector.

The FSUSB63 has a break-before-make time to force re-enumeration by the host when switching between different HS USB 2.0 controllers and thus requires minimal software changes.

The FSUSB63 is compliant with the requirements of USB 2.0 and features extremely low on capacitance (C<sub>ON</sub>). The wide bandwidth exceeds the requirement to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

## Related Resources

- For samples and questions, please contact: [Analog.Switch@fairchildsemi.com](mailto:Analog.Switch@fairchildsemi.com).
- FSUSB63 Demonstration Board

## Typical Application

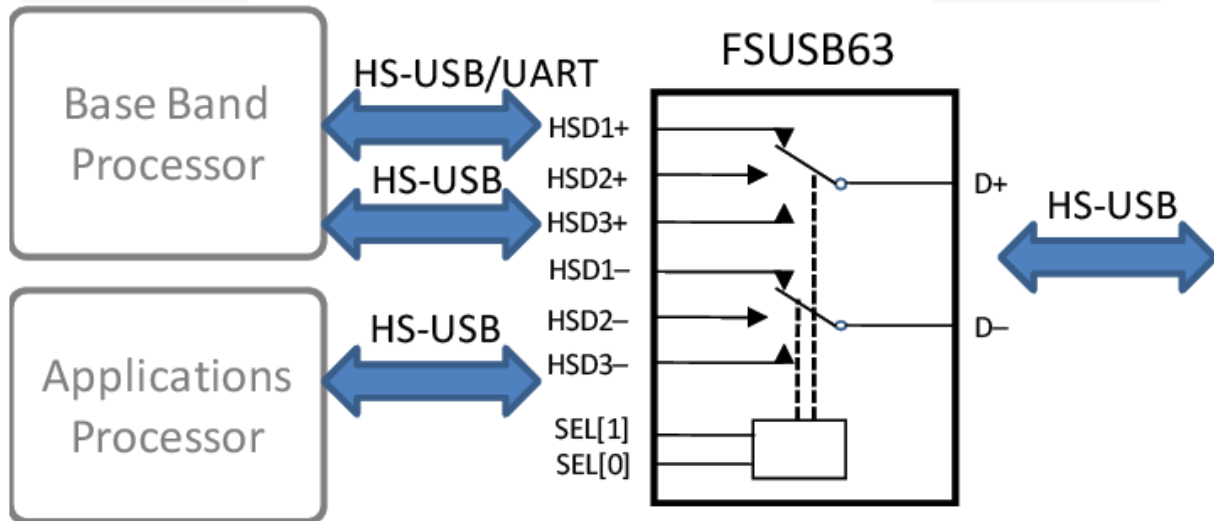


Figure 1. Analog Symbol

## Pin Configuration

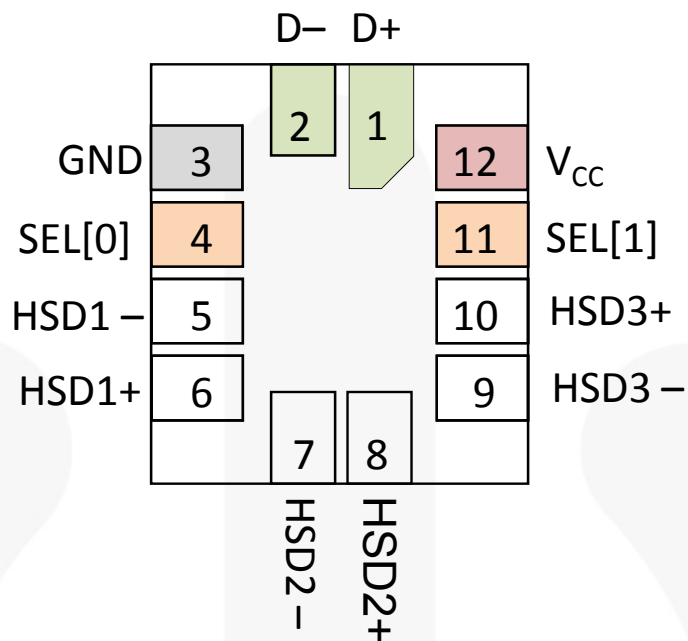


Figure 2. Pin Assignments (Top Through View)

## Pin Descriptions

Pin #	Name	Description
1	D+	USB 2.0 High Speed or Full Speed Data Bus D+
2	D-	USB 2.0 High Speed or Full Speed Data Bus D-
3	GND	Ground
4	SEL[0]	Path Selection Control Inputs ( <i>see functional table below</i> )
5	HSD1-	Multiplexed First Source Path for D-
6	HSD1+	Multiplexed First Source Path for D+
7	HSD2-	Multiplexed Second Source Path for D-
8	HSD2+	Multiplexed Second Source Path for D+
9	HSD3-	Multiplexed Third Source Path for D-
10	HSD3+	Multiplexed Third Source Path for D+
11	SEL[1]	Path Selection Control Inputs ( <i>see functional table below</i> )
12	V <sub>CC</sub>	Supply Voltage

## Functional Table

Mode	SEL[1]	SEL[0]	Function
Sleep Mode	0	0	D+, D- Switch Paths Open
USB Port 1	0	1	D+=HSD1+, D-=HSD1-
USB Port 2	1	0	D+=HSD2+, D-=HSD2-
USB Port 3	1	1	D+=HSD3+, D-=HSD3-

## Eye Compliance

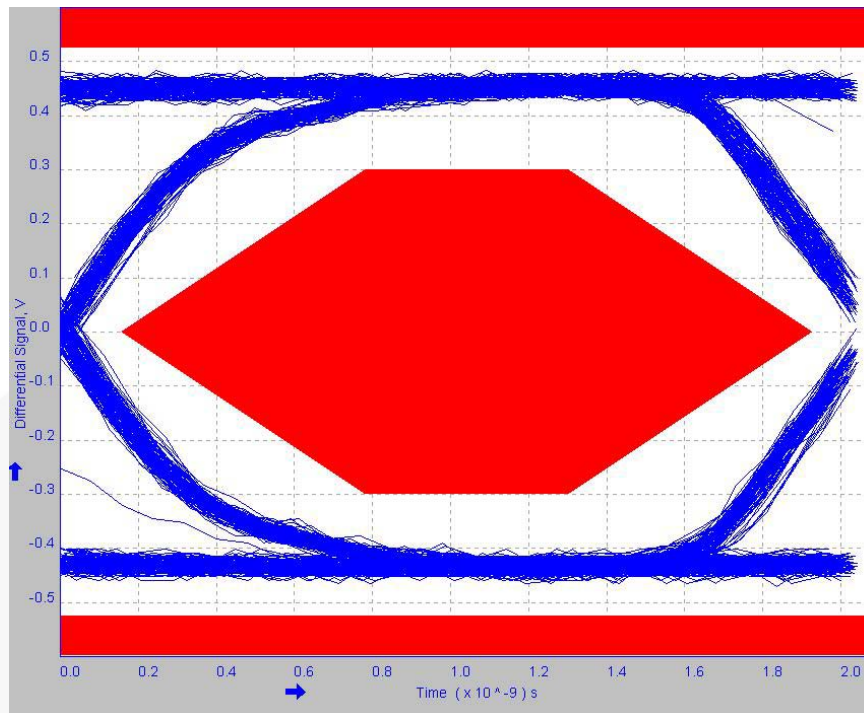


Figure 3. USB 2.0 HS-USB Eye Compliance Pass Through (without Switch)

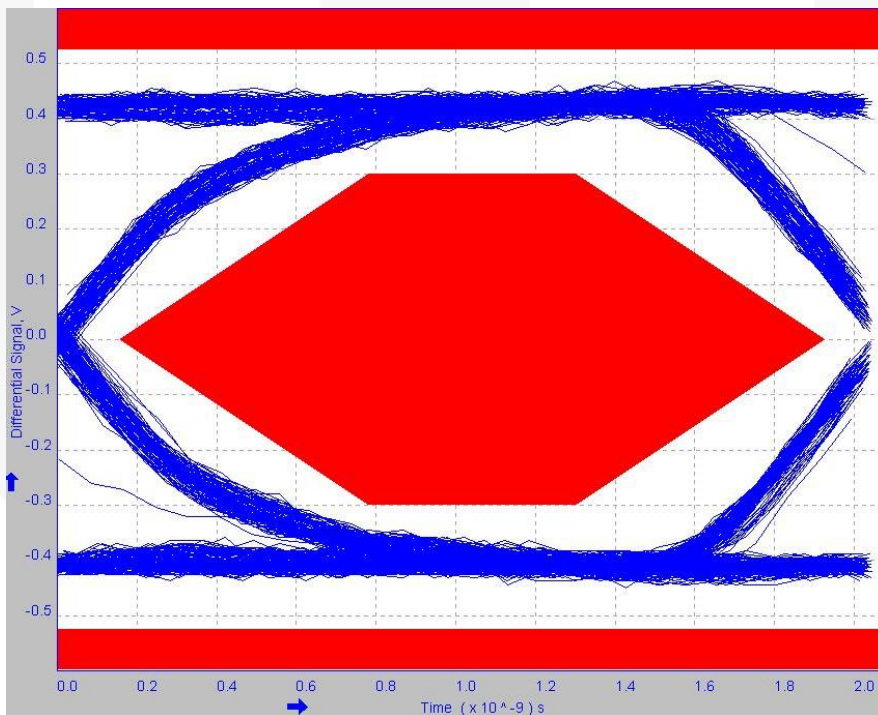


Figure 4. USB 2.0 HS-USB Eye Compliance with Switch

### Notes:

1. Figure 3 indicates the HS-USB eye compliance of the source across a characterization board prior to the implementation of the switch.
2. Figure 4 shows the total impact the switch has on HS-USB eye compliance when compared to Figure 3

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
V <sub>CC</sub>	Supply Voltage	-0.50	5.25	V	
V <sub>CNTRL</sub>	DC Input Voltage (SEL[1:0]) <sup>(3)</sup>	-0.5	V <sub>CC</sub>	V	
V <sub>SW</sub>	DC Switch I/O Voltage <sup>(3)</sup>	-0.50	5.25	V	
I <sub>IK</sub>	DC Input Diode Current	-50		mA	
I <sub>OUT</sub>	DC Switch Current		50	mA	
T <sub>STG</sub>	Storage Temperature	-65	+150	°C	
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)		1	Level	
ESD	IEC61000-4-2 System on USB Connector Pins D+ & D-	Air Gap	15.0		kV
		Contact	8.0		
	Human Body Model, JEDEC: JESD22-A114	Power to GND	16.0		
		I/O to GND	5.0		
		All Pins	5.0		
Charged Device Model, JEDEC: JESD22-C101	1.5				

### Note:

3. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	2.7	4.4	V
V <sub>CNTRL</sub> <sup>(4)</sup>	Control Input Voltage (SEL[1:0])	0	V <sub>CC</sub>	V
V <sub>SW</sub>	Switch I/O Voltage	-0.5	4.3	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C

### Note:

4. The control input must be held HIGH or LOW and it must not float.

## DC Electrical Characteristics

All typical values are for  $V_{CC}=3.3V$  at  $T_A=25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Units
				Min.	Typ.	Max.	
$V_{IK}$	Clamp Diode Voltage	$I_{IN}=-18mA$	2.7			-1.2	V
$V_{IH}$	Input Voltage High	SEL[1], SEL[0] Inputs	2.7 to 4.3	1.0			V
$V_{IL}$	Input Voltage Low	SEL[1], SEL[0] Inputs	2.7 to 4.3			0.35	V
$I_{IN}$	Control Input Leakage	All Combinations of SEL[1] & SEL[0] in the Truth Table (LOW=0V & HIGH= $V_{CC}$ )	4.3			1	$\mu A$
$I_{OZ}$	Off-State Leakage	$0 \leq D_n, HSD1_n, HSD2_n, HSD3_n \leq 3.6V$	4.3	-2		2	$\mu A$
$I_{OFF}$	Power-Off Leakage Current (All I/O Ports)	$V_{SW}=0V$ to $4.3V$ , $V_{CC}=0V$ , Figure 7	0	-2		2	$\mu A$
$R_{ON}^{(5)}$	HS Switch On Resistance	$V_{SW}=0.4V$ , $I_{ON}=-8mA$ , Figure 6	3.0		6.0	7.8	$\Omega$
$\Delta R_{ON}$	HS Delta $R_{ON}^{(6)}$	$V_{SW}=0.4V$ , $I_{ON}=-8mA$	3.0		0.50		$\Omega$
$I_{CCSLP}$	Sleep Mode Supply Current	SEL[1]=SEL[0]=0	3.6			1	$\mu A$
$I_{CCACT}$	Active Mode Supply Current	$V_{CNTRL}=0$ or $V_{CC}$ , $I_{OUT}=0$	2.7		7.5	15.0	$\mu A$
			3.6		8.5	16.0	$\mu A$
$I_{CCT}$	Increase in $I_{CC}$ Current per Control Input and $V_{CC}$	$V_{CNTRL}=1.8V$	3.6		1.5	4.0	$\mu A$
		$V_{CNTRL}=1.2V$	3.6		3.0	5.0	$\mu A$

### Notes:

- Measured by the voltage drop between  $HSD_n$  and  $D_n$  pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two ( $HSD_n$  or  $D_n$  ports).
- Guaranteed by characterization.

## AC Electrical Characteristics

All typical values are for  $V_{CC}=3.3V$  at  $T_A=25^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Units
				Min.	Typ.	Max.	
$t_{ON}$	Turn-On Time when Switching from One USB Path (or Disabled i.e. SEL=00) to Another USB Path	$R_L=50\Omega$ , $C_L=35pF$ $V_{SW}=0.8V$ Figure 8, Figure 9	3.0 to 3.6	126		400	$\mu s$
$t_{OFF}$	Turn-Off Time SEL $\neq$ 00 (Any of the Three USB Paths Active) to SEL=00 (Disabled)	$R_L=50\Omega$ , $C_L=35pF$ $V_{SW}=0.8V$ Figure 8, Figure 9	3.0 to 3.6			45	ns
$t_{PD}$	Propagation Delay <sup>(7)</sup>	$C_L=5pF$ , $R_L=50\Omega$ Figure 8, Figure 10	3.3		0.25		ns
$t_{BBM}$	Break-Before-Make Time	$R_L=50\Omega$ , $C_L=35pF$ $V_{SW1}=V_{SW2}=0.8V$ , Figure 12	3.0 to 3.6	126		400	$\mu s$
$O_{IRR}$	Off Isolation <sup>(7)</sup>	$R_L=50\Omega$ , $f=240MHz$ Figure 14	3.0 to 3.6		-42		dB
Xtalk	Non-Adjacent Channel Crosstalk <sup>(7)</sup>	$R_L=50\Omega$ , $f=240MHz$ Figure 15	3.0 to 3.6		-33		dB
BW	-3db Bandwidth <sup>(7)</sup>	$R_L=50\Omega$ , $C_L=0pF$ Figure 13	3.0 to 3.6			830	MHz
		$R_L=50\Omega$ , $C_L=5pF$ Figure 13	3.0 to 3.6			510	MHz

### Note:

- Guaranteed by characterization.

## USB High-Speed Related AC Electrical Characteristics

Symbol	Parameter	Conditions	Vcc (V)	TA=- 40°C to +85°C			Units
				Min.	Typ.	Max.	
$t_{SK(P)}$	Pulse Skew <sup>(8)</sup>	$V_{SW}=0.2V_{diffPP}$ , Figure 11, $C_L=5pF$	3.0 to 3.6		10		ps
$t_{SK(I)}$	Skew Between Differential Signals within a Pair <sup>(8)</sup>	$V_{SW}=0.2V_{diffPP}$ , Figure 11, $C_L=5pF$	3.0 to 3.6		10		ps

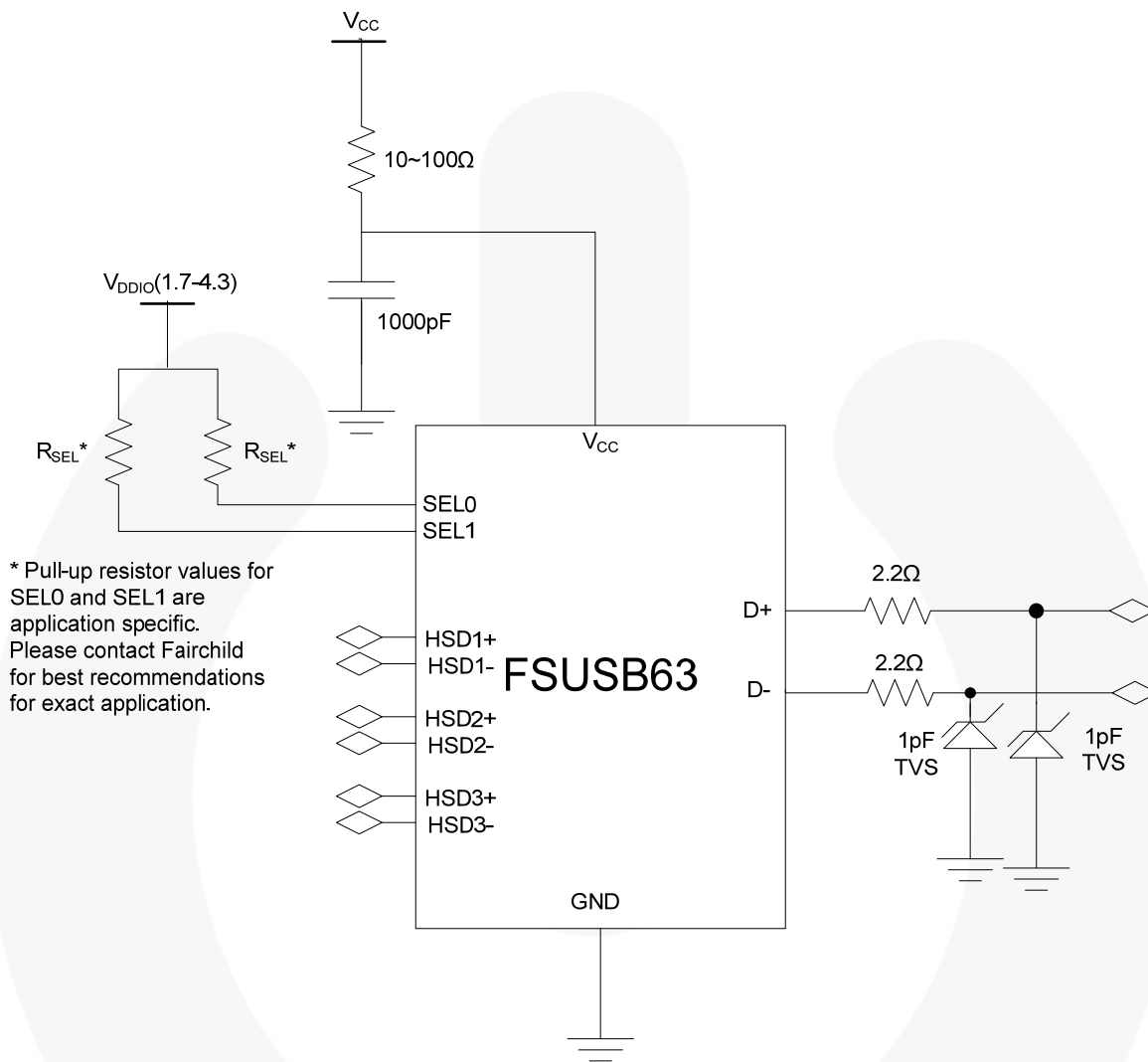
## Capacitance

Symbol	Parameter	Conditions	TA=- 40°C to +85°C			Units
			Min.	Typ.	Max.	
$C_{iN}$	SEL[1:0] Input Capacitance <sup>(8)</sup>	$V_{CC}=0V$		3		pF
$C_{ON}$	D+/D- On Capacitance <sup>(8)</sup>	$V_{CC}=3.3V$ , Any of the Three Switch Paths Enabled, $f=1MHz$ , Figure 17		6		
		$V_{CC}=3.3V$ , Any of the Three Switch Paths Enabled, $f=240MHz$ <sup>(9)</sup>		5		
$C_{OFF}$	HSD1 <sub>n</sub> , HSD2 <sub>n</sub> , HSD3 <sub>n</sub> Off Capacitance <sup>(8)</sup>	$V_{CC}=0V$ or ( $V_{CC}=3.3V$ and SEL[1]=SEL[0]=0V) Figure 16		2		

### Notes:

8. Guaranteed by characterization.
9. Effective capacitance measured on a network analyzer.

### Reference Schematic



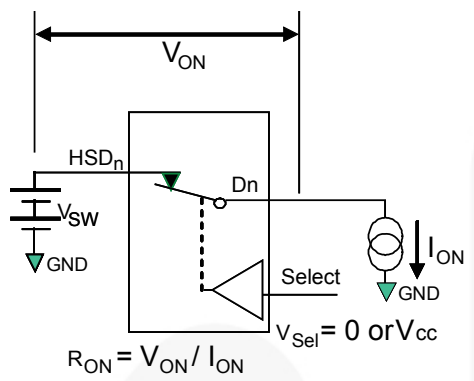
\* Pull-up resistor values for SEL0 and SEL1 are application specific. Please contact Fairchild for best recommendations for exact application.

Figure 5. Reference Schematic

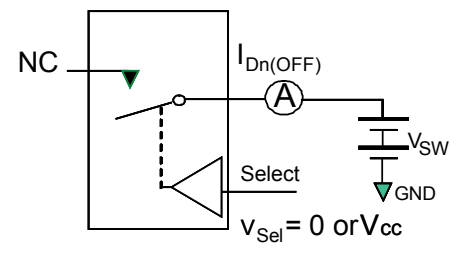




**Test Diagrams**

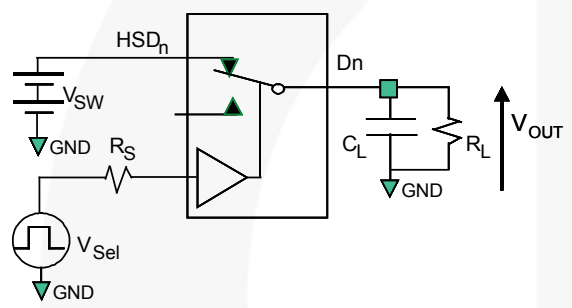


**Figure 6. On Resistance**



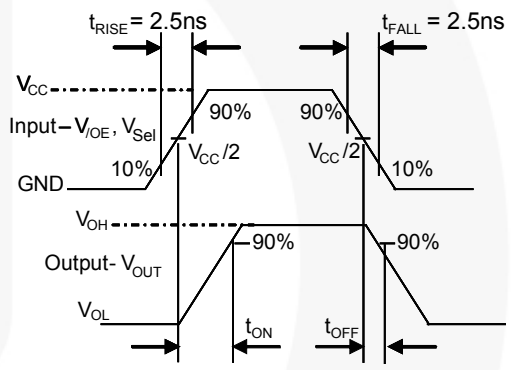
\*\*Each switch port is tested separately

**Figure 7. Off Leakage**

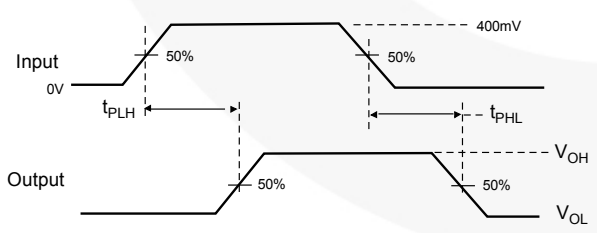


$R_L$ ,  $R_S$ , and  $C_L$  are functions of the application environment (see AC Tables for specific values)  
 $C_L$  includes test fixture and stray capacitance.

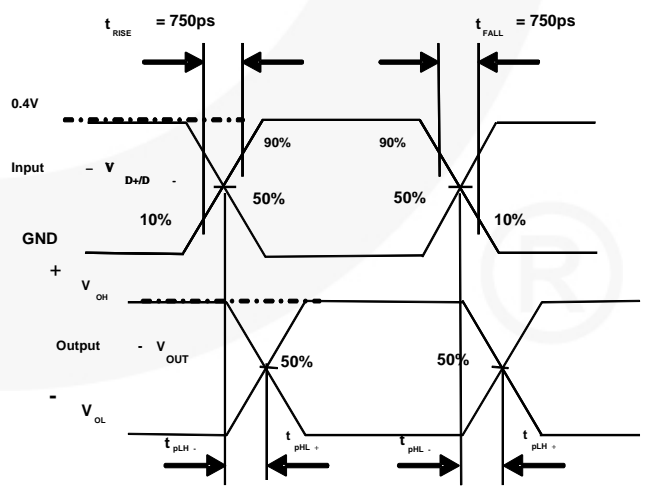
**Figure 8. AC Test Circuit Load**



**Figure 9. Turn-On / Turn-Off Waveforms**



**Figure 10. Propagation Delay ( $t_{rF} - 500ps$ )**

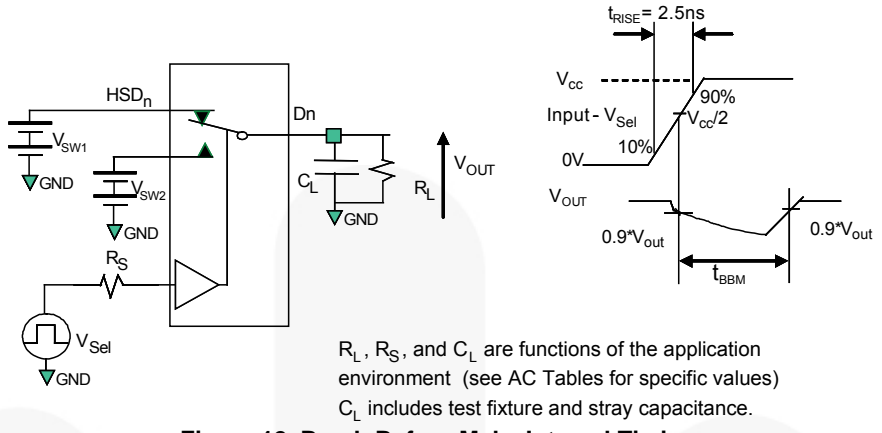


**Figure 11. Skew Test Waveforms**

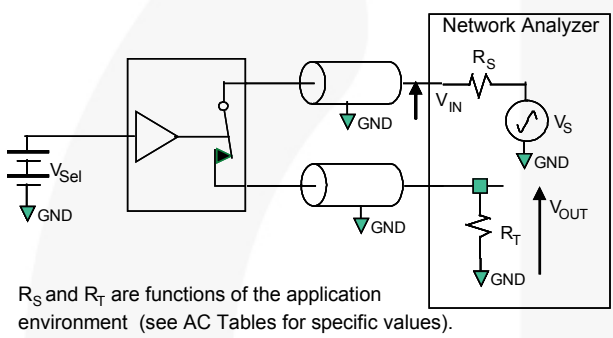
$$t_{SK(P)} = |t_{PLH-} - t_{PHL-}| \text{ or } |t_{PLH+} - t_{PHL+}|$$

$$t_{SK(I)} = |t_{PLH-} - t_{PHL+}| \text{ or } |t_{PLH+} - t_{PHL-}|$$

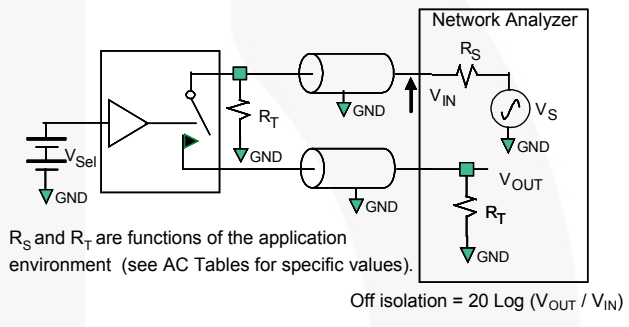
**Test Diagrams (Continued)**



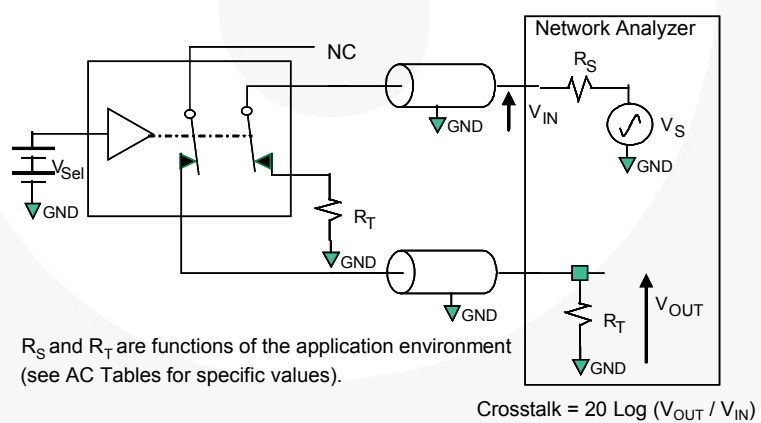
**Figure 12. Break-Before-Make Interval Timing**



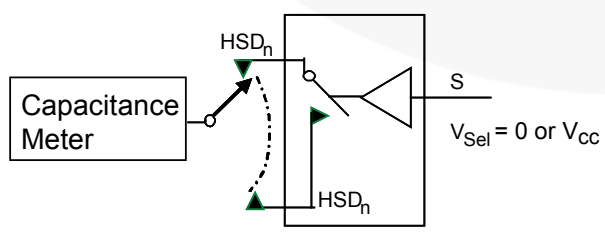
**Figure 13. Bandwidth**



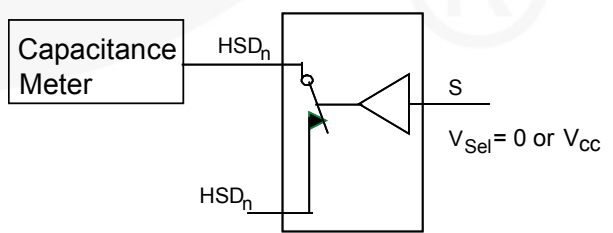
**Figure 14. Channel Off Isolation**



**Figure 15. Non-Adjacent Channel-to-Channel Crosstalk**

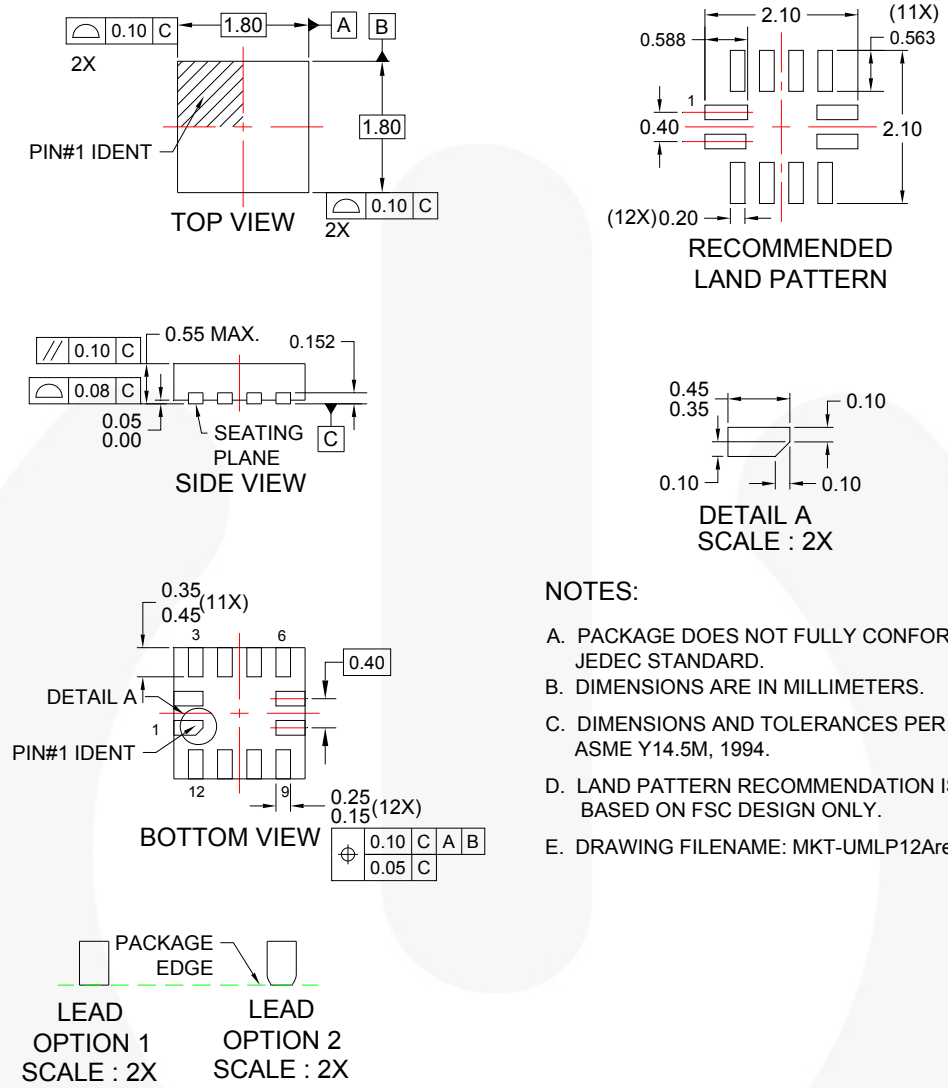


**Figure 16. Channel Off Capacitance**



**Figure 17. Channel On Capacitance**

### Physical Dimensions



- NOTES:**
- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  - D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
  - E. DRAWING FILENAME: MKT-UMLP12Arev4.

**Figure 18. 12-Lead, Ultrathin Molded Leadless Package (UMLP)**

### Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSUSB63UMX	KG	-40 to +85°C	12-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.8mm x 1.8mm x 0.55mm, 0.4mm pitch




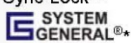
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| BitSiC™  | GreenBridge™                                   | QFET®  | TinyBuck™   |
| Build it Now™  | Green FPS™                                     | QS™  | TinyCalc™   |
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| CROSSVOLT™   | GTO™   |  ™                | TinyPower™  |
| CTL™   | IntelliMAX™                                    | Saving our world, 1mW/W/kW at a time™  | TinyPWM™  |
| Current Transfer Logic™  | ISOPLANAR™                                     | SignalWise™  | TinyWire™   |
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|  Fairchild® | MicroPak2™                                     | SuperFET®  | UHC®  |
| Fairchild Semiconductor®   | MillerDrive™                                   | SuperSOT™-3  | Ultra FRFET™  |
| FACT Quiet Series™   | MotionMax™                                     | SuperSOT™-6  | UniFET™   |
| FACT®  | mWSaver™                                       | SuperSOT™-8  | VCX™  |
| FAST®  | OptoHiT™                                       | SupreMOS®  | VisualMax™  |
| FastvCore™   | OPTOLOGIC®                                     | SyncFET™   | VoltagePlus™  |
| FETBench™  | OPTOPLANAR®                                    | Sync-Lock™   | XS™   |
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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